Datasheet

MAROC 3A

MAROC3A is a 64-channel chip designed to readout negative fast input current pulses such as those provided by Multi Anode Photo Multipliers. Each channel provides a 100% trigger rate for signal greater than 1/3 photoelectron (50fC) and a charge measurement up to 30 photoelectrons (~ 5 pC) with a linearity of 2%. The gain of each channel can be tuned between 0 and 4 thanks to an 8 bit variable gain preamplifier allowing to compensate the non- uniformity between detector channels. A slow shaper combined with two Sample and Hold capacitors allows storing the charge up to 5 pC as well as the baseline. In parallel, 64 trigger outputs are obtained thanks to two possible trigger paths: one made of a bipolar or unipolar fast (15 ns) shaper followed by one discriminator for the photon counting and one made with a bipolar fast shaper (with a lower gain) followed by a discriminator to deliver triggers for larger input charges (> 1 pe). The discriminator thresholds are set by two internal 10-bit DACs. A digital charge output is provided by an integrated 8, 10 or 12 bit ADC Wilkinson. 828 Slow Control parameters allow versatility and various settings.

Figure 1 – Maroc 3A

Parameter	Value
Detector Read-Out	MAPMT, SiPM
Number of Channels	64
Signal Polarity	Negative
Sensitivity	Trigger on 1/3 photo-electron or 50 fC with a 10^6 PM gain
Timing Resolution	60ps RMS on single photo-electron, Threshold 1/3 of photo-electron
Dynamic Range	5 pC (10^6 PM gain), Integral Non Linearity: 2% up to 5 pC
Packaging & Dimension	PQFP240,TFBGA353, Naked die 4 x 3.9 mm ~ 16 mm^2
Power Consumption	3.5 mW /ch, power supply= 3.3V
Inputs	64 current inputs
Outputs	64 trigger outputs Wired OR of the 64 triggers for each of the 2 discriminators 1 multiplexed analog charge output that can be daisy chained 1 digital charge measurement (8, 10 or 12 bits)
Internal Programmable Features	gain adjustment between 0 and 4 over 8 bits for each input preamp, trigger threshold adjustment (10bits), analog and digital charge measurement, 64 trigger outputs, 64 trigger masks

Table 1 – ASIC main parameters

Learn more about MAROC3A

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1 General description

MAROC3A is 64-channel Multi-Anode Photomultiplier (MAPMT) readout chip, suitable for application requiring signal triggering and charge measurements. This chip offers triggering threshold down to 50 fC, 64-channel trigger outputs and charge measurement via internal ADC.

Main features of this ASIC are the following:

- 64-chanel low impedance pre-amplifier with a variable 8-bit gain for each channel. This variable gain allows compensating the MAPMT gain dispersion up to a factor of 4.
- 64 trigger outputs coming from the fast shapers and its associated discriminator. Triggering line could come from either a fast shaper for low signal threshold (50 fc or lower) or a bipolar fast shaper with lower pre-amp gain for higher charge input charge discrimination. The thresholds are set by two internal 10 bit-DACs.
- 64-channel variable peaking time slow shaper (30-150ns) followed by two Track and Hold circuits providing multiplexed analog charge output from baseline up to 15pC.
- Charge measurement can also be performed internally by ADC Wilkinson (8/10/12 bits)

The pin or ball-out numbering used throughout this document can be referred in Table 15, Figure 33, Figure 34, Figure 35 and Figure 36.

The ASIC presented in this document is an update of MAROC3 and update is listed in Section 9.

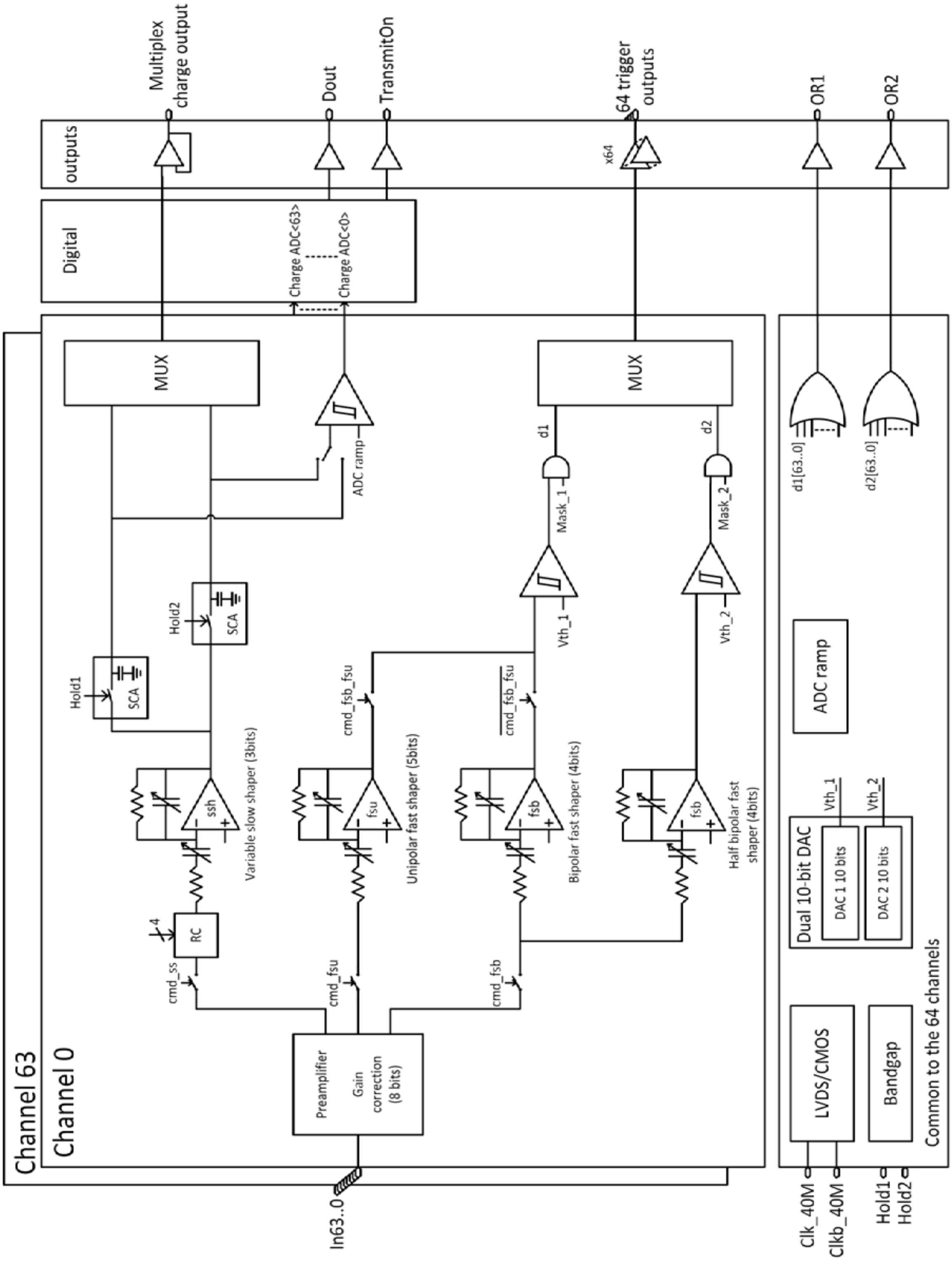


Figure 2 - General ASIC block scheme

2 Operation modes

This ASIC can be operated in various configurations such as in fully analog or mixed-signal mode. In fully analog operation, external digital signals are not required except for initial configuration. Once the chip is configured, it will be operating continuously without interruption. In analog mode, two applications can be foreseen : signal triggering and charge measurement. In mixed-signal mode, only charge measurement can be performed and it is done via internal ADC.

2.1 Analog Triggering

In this mode, 64 trigger outputs are available directly on the ASIC pads for each channel. The trigger can be selected from several fast shapers that are available on this chip. The threshold level can be set down to one-third photoelectron (for 1e^{6} detector gain). The trigger outputs can be masked individually through initial Slow Control configuration. Trigger outputs can be used in various applications such as photon counting, time measurement via external TDC or detector triggering.

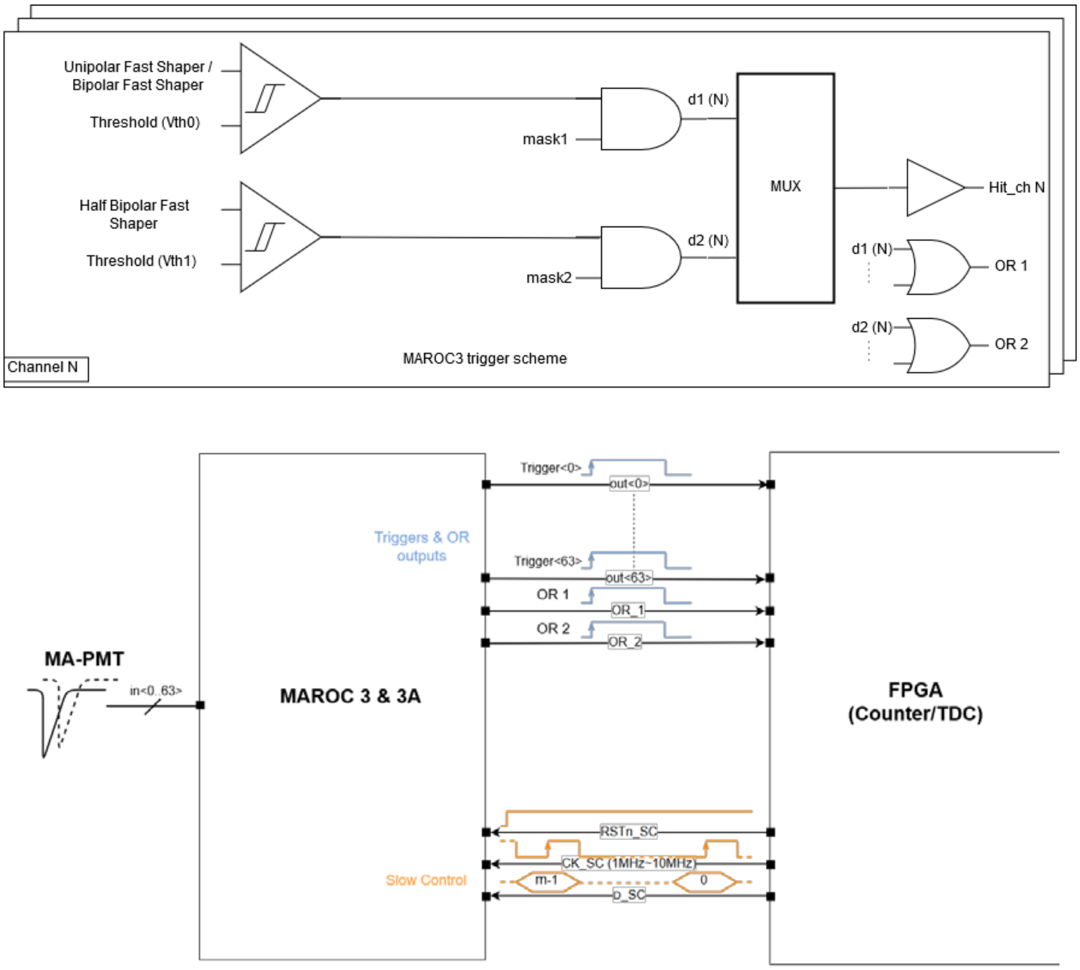


Figure 3 – Maroc3 & 3A trigger scheme and analog trigger application example

2.2 Analog Charge measurement

Analog charge measurement is available through an analog signal multiplexer. User can sequentially scan the slow shaper output for each channel. A set of internal register (Read register) is available in order to shift through all the slow shaper output multiplexer. In order to use this multiplexer output in conjunction with an external ADC, two Hold inputs are also available on this this ASIC so that the slow shaper amplitude can be sampled and saved to the internal analog memories (Switch Capacitor Array – SCA) before the signal conversion.

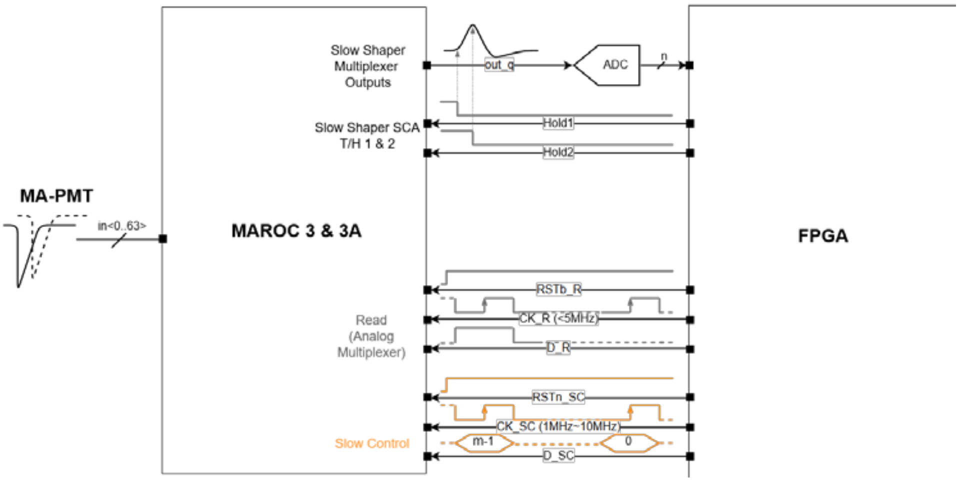


Figure 4 - Analog Charge measurement

2.3 Mixed-signal mode charge measurement

In this mode, the charge measurement is performed directly with the ADC embedded in the ASIC. Even though this ADC conversion rate is relatively modest, it still offers an excellent linearity and high resolution up to 12 bits. Similarly, like the charge measurement in analog mode, the Hold signal (there are two inputs in this ASIC) has to be provided externally in order to sample the slow shaper output. Once the slow shaper signal is held correctly, the digital conversion can be initiated through a dedicated digital input (start_ADC). The data will be then transferred through a serial output. The conversion rate vary between 8 kEvents/s and 53 kEvents/s depending on the chosen ADC resolution.

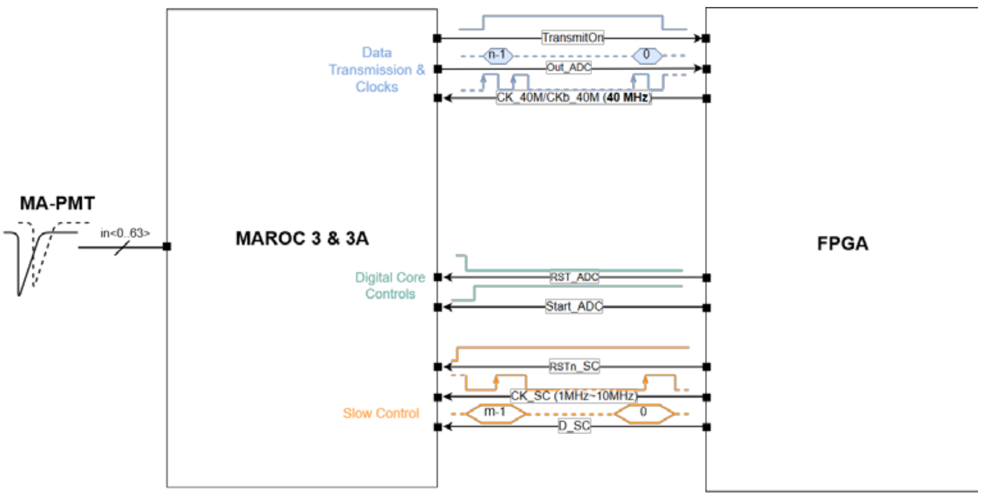


Figure 5 – Mixed-signal charge measurement example

3 ASIC front-end

3.1 Pre-amplifier

The pre-amplifier of MAROC3 chip is composed of a common base amplifier followed by a set of current mirror. A variation of the common base circuit known as "super common base" is employed here in order to provide low input impedance (50~100Ω) and low offset with a minimal power consumption. Then a set of current mirror is used for copying and distributing the current to charge measurement and trigger shapers in this ASIC. Thanks to this current mirror, user could tune the current copying gain by modifying the current mirror ratio (0~4) individually for each channel. This feature can be used to compensate the non-uniformity of each detector channel. The input signal polarity is required to be negative.

For controlling the current copy gain (Variable Gain in Figure 6) can be adjusted through Slow Control bit #190 - 764. Characteristic of this current copy gain is the following :

- Resolution : 8-bit – BCD coded
- Max gain : 3.984
- Min gain : 0
- Step : 0.0156/LSB

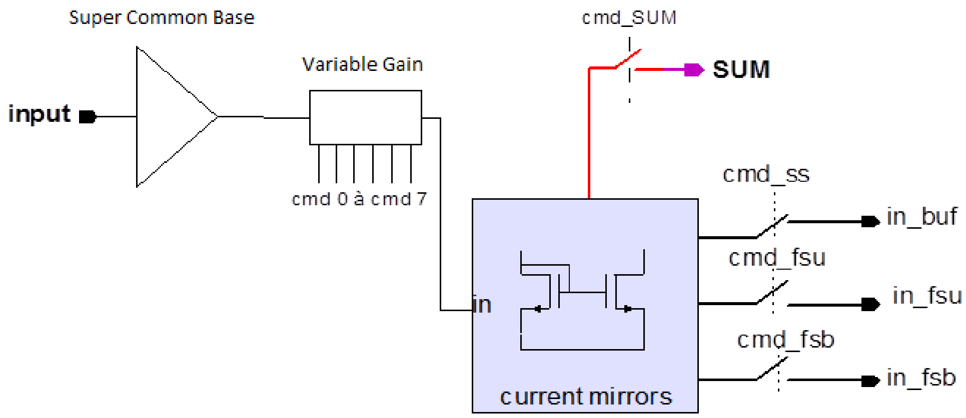


Figure 6 - Pre-amplifier block diagram

The pre-amplifier signal can be sent to various fast shapers for generating trigger and slow shaper for charge measurement via Slow Control :

- cmd_fsb: Slow Control bit #186 – Pre-amplifier signal is sent to Bipolar Fast Shaper and Half Bipolar Fast Shaper for triggering. Additional Slow Control configuration is required for trigger selection except for trigger for Half Bipolar Fast Shaper (refer to Section 3.2).
- cmd_fsu: Slow Control bit #188 – Pre-amplifier signal is sent to Unipolar Fast Shaper for triggering. Additional Slow Control configuration is required for trigger selection (refer to Section 3.2)
- cmd_ss: Slow Control bit #187 – Pre-amplifier signal is sent to Slow Shaper for charge measurement (refer to Section 3.3).

3.1.1 Sum outputs

There is a possibility to sum up to eight adjacent pre-amplifier channels together. In total there 8 sum outputs covering the 64-channel pre-amplifier. The sum output can be enabled individually in each channel (cmd_sum i … cmd_sum i+7 in Figure 7) through Slow Control located between bit #189 to bit #756. Refer to Table 12 for exact location of these bits of each channel.

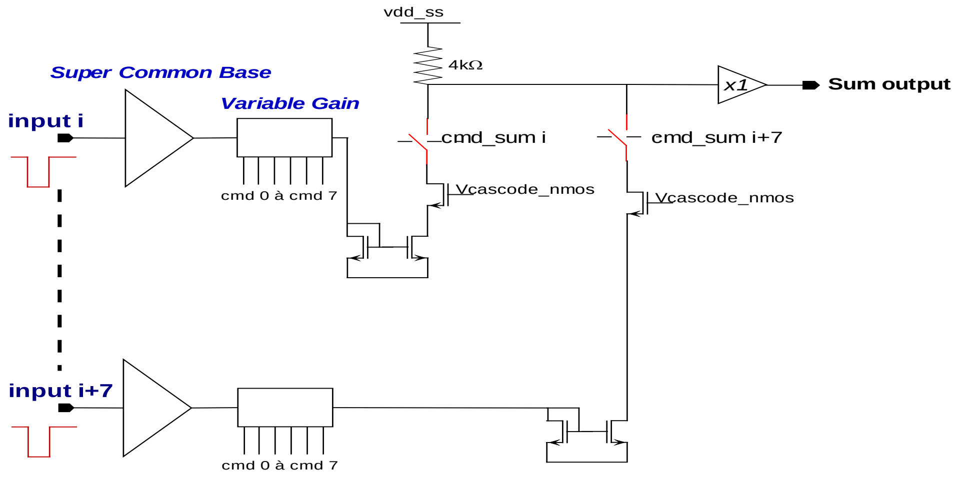


Figure 7 - Pre-amplifier sum output

3.2 Fast shapers

For the input triggering, there are three different shapers available for user to choose. The available shapers are the following : Unipolar Fast Shaper, Bipolar Fast Shaper and Half Bipolar Fast Shaper. Depending on the shaper chosen, this chip could trigger signal from 50fC (1/3 photoelectron for $1e^6$ detection gain).

Unipolar Fast shaper is suitable for triggering the input signal down to 50 fC or lower.

When Bipolar Fast Shaper is chosen for triggering line, the input charge is expected to be much higher. For this triggering line, it is advised that the pre-amplifier current copying gain to be reduced in order to avoid saturation. For both Bipolar Fast Shaper and Half Bipolar Fast Shaper, the design and parameters are identical. The term "Half" is added to signify that the pre-amplifier gain is being halved systematically (divided by 2) before the signal is fed to Half Bipolar Fast Shaper.

User could choose to tune the feedback capacitors and resistors of each fast shaper shown in Figure 8.

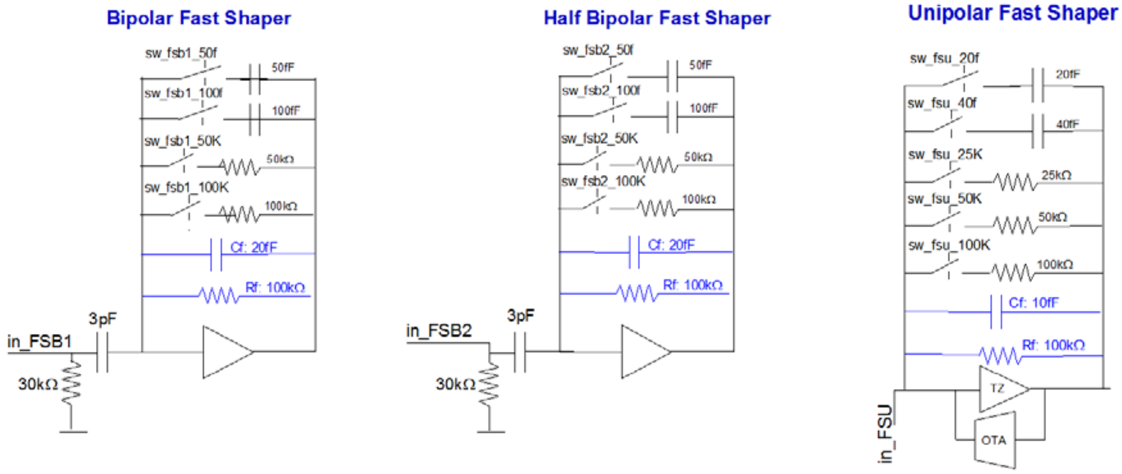


Figure 8 - Fast shapers block diagram : Bipolar Fast Shaper (Left), Half Bipolar Fast Shaper (Middle) & Unipolar Fast Shaper (Right).

For Bipolar & Half Bipolar Fast Shaper, the feedback resistor and capacitor values can be selected between 25k Ohm to 100 k Ohm and between 20fF to 170fF respectively via Slow Control parameters. The resulting time constant, *tau*, is between 0.5 ns and 17 ns. Feedback resistor and capacitor of Bipolar Fast Shaper/Half Bipolar Fast Shaper can be assessed at the following Slow Control bits:

- Feedback capacitor – sw_fsb1_50f (SC #167) & sw_fsb1_100f (SC #168) for Bipolar Fast Shaper.
  – sw_fsb2_50f (SC #161) & sw_fsb2_100f (SC #162) for Half Bipolar Fast Shaper.
- Feedback resistor – sw_fsb1_50k (SC #170) & sw_fsb1_100k (SC #169) for Bipolar Fast Shaper.
  – sw_fsb2_50k (SC #164) & sw_fsb2_100k (SC #163) for Half Bipolar Fast Shaper.

sw_fsb1(2)_100f & sw_fsb1(2)_50f	Feedback Capacitor	sw_fsb1(2)_100k & sw_fsb1(2)_50k	Feedback Resistor
"00"	20fF	"00"	100k Ohm
"01"	70fF	"01"	33k Ohm
"10"	120fF	"10"	50k Ohm
"11"	170fF	"11"	25k Ohm

Table 2 - Bipolar and Half Bipolar shapers feedback resistor and capacitor selection through Slow Control

The characteristics of the Bipolar Fast Shaper are listed in the following tables (pre-amplifier gain is set at unity value):

<table>
<tr><th colspan="2" rowspan="2">Gain[1] (mV/p.e) | Time constant</th><th colspan="4">Feedback Capacitor</th></tr>
<tr><th>20f F</th><th>70f F</th><th>120f F</th><th>170f F</th></tr>
<tr><td rowspan="4">Feedback Resistor</td><td>25k Ohm</td><td>N/A | 0.5 ns</td><td>N/A | 1.75 ns</td><td>N/A | 3 ns</td><td>211 mV/p.e | 4.25 ns</td></tr>
<tr><td>33k Ohm</td><td>N/A | 0.66 ns</td><td>N/A | 2.31 ns</td><td>N/A | 3.96 ns</td><td>250mV/p.e | 5.61 ns</td></tr>
<tr><td>50k Ohm</td><td>N/A | 1 ns</td><td>N/A | 3.5 ns</td><td>N/A | 6 ns</td><td>302 mV/p.e | 8.5 ns</td></tr>
<tr><td>100k Ohm</td><td>N/A | 2 ns</td><td>N/A | 7 ns</td><td>N/A | 12 ns</td><td>371 mV/p.e | 17ns</td></tr>
</table>

Table 3 - Gain and time constant for Bipolar Fast Shaper

[1] Gain for Half Bipolar Fast Shaper is not fully measured, but it is expected to be about half of the measured gain for Bipolar Fast Shaper reported in the Table 3.

Unipolar Fast Shaper adjustment is also done via Slow Control and user can configure the feedback capacitor/resistor of this shaper. The values of the feedback component can be set through the following Slow Control bits:

- Feedback capacitor – sw_fsu_20f (SC #175) & sw_fsu_40f (SC #174) for Unipolar Fast Shaper.

- Feedback resistor – sw_fsu_25k (SC #173), sw_fsu_50k (SC #172) & sw_fsu_100k (SC #171) for Unipolar Fast Shaper.

sw_fsu_40f & sw_fsu_20f	Feedback Capacitor	sw_fsu_100k, sw_fsu_50k & sw_fsu_25k	Feedback Resistor
"00"	10fF	"000"	100k Ohm
"01"	30fF	"001"	20k Ohm
"10"	50fF	"010"	33k Ohm
"11"	70fF	"011"	14k Ohm
		"100"	50k Ohm
		"101"	16k Ohm
		"110"	25k Ohm
		"111"	12.5k Ohm

Table 4 – Fast Unipolar Shaper feedback resistor and capacitor selection through Slow Control

The characteristics of the Unipolar Fast Shaper for selected configuration are listed in the following tables (pre-amplifier gain is set at unity value):

Gain (mV/p.e) | Time constant		Feedback Capacitor			
		10f F	30f F	50f F	70f F
Feedback Resistor	12.5k Ohm	N/A | 0.12 ns	N/A | 0.36 ns	N/A | 0.6 ns	8 mV/p.e | 0.9 ns
	14k Ohm	N/A | 0.14 ns	N/A | 0.4 ns	N/A | 0.7 ns	9.6 mV/p.e | 0.98 ns
	50k Ohm	N/A | 0.5 ns	N/A | 1.5 ns	N/A | 2.5 ns	192 mV/p.e | 3.5 ns
	100k Ohm	N/A | 1 ns	N/A | 3 ns	N/A | 5 ns	720 mV/p.e | 7 ns

Table 5 - Gain and time constant for Bipolar Fast Shaper

3.2.1 Trigger scheme

Assuming that the pre-amplifier output has been set accordingly, up to two triggers can be generated simultaneously in a channel before selecting which to trigger to be sent on the ASIC pin. For the first trigger, D1 in Figure 9, user can select through Slow Control between the signal from Unipolar Fast Shaper or Bipolar Fast Shaper to be sent to the discriminator:

- cmd_fsb_fsu : Slow Control bit #166 – Set this bit to '1' for Unipolar Fast Shaper or '0' for Bipolar Fast Shaper

The second trigger, D2 in Figure 9, comes solely from Half Bipolar Fast Shaper. Similarly, the threshold can be set independently for each trigger through Slow Control : VTH0(DAC0) for D1 trigger and VTH1(DAC1) for D2 trigger. Characteristics these thresholds are the following :

	VTH0(DAC0)		VTH1(DAC1)
Slow Control	#13(MSB)-#22(LSB)		#3(MSB)-#12(LSB)
Resolution	10-bit		10-bit
SC #2 – small_dac	'0' – Disable	'1' - Enable	N/A
Max output (Code=0)	2.3V	2.3V	2.3V
Min output (Code =1023)	6mV	1.2V	-4mV
LSB	2.2mV	1.1mV	2.3mV

Table 6- Trigger threshold characteristics

Additionally, as shown in Table 6, there is a Slow Control parameter (bit #2 – small_dac) with will divide the LSB of VTH0 by roughly 2 in order to get a better precision at setting the threshold for D1 trigger.

As all the fast shapers signal are expected to be discriminated at positive polarity, users are expected to set the trigger threshold higher than the baseline (refer to Table 7). The correct threshold will vary according to the configuration of the fast shapers and pre-amplifier described in previous section.

	Bipolar Fast Shaper	Half Bipolar Fast Shaper	Unipolar Fast Shaper
Measured baseline	1.93 V	1.93 V	1 V
Baseline equivalent in DAC Unit	353 (VTH0 – SC#2 – small_DAC ='1')	169 (VTH1)	569 (VTH0 – SC#2 – small_DAC ='0')

Table 7 - Trigger Threshold baseline for fast shapers

Masking option is available for all of the two triggers. This setting can be set for each channel and each trigger through Slow Control bits # 27-154.

The trigger output for each channel is available on out<0…63> pins on various location either on the CDQP240 or BGA353 packaging – refer to Section 8 for the locations. Only one of the D1 and D2 triggers can be sent out at one time, and this selection is done through Slow Control :

- d1_d2 : Slow Control bit #156 – Set this bit to '0' for D1 and '1' for D2

Additionally, the D1 and D2 triggers are regrouped by 64-input OR gate at the following locations:

- OR 1 : pin 191/B16 – OR64 for D1 trigger
- OR 2 : pin 192/B17 – OR64 for D2 trigger

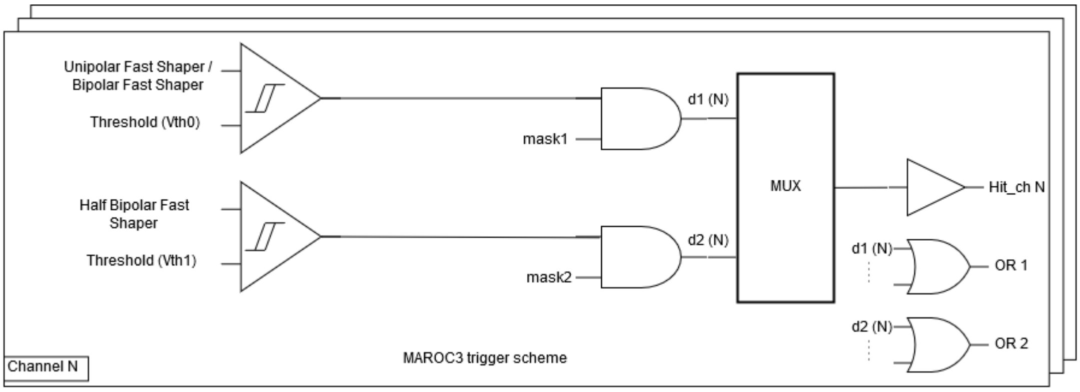


Figure 9 - Trigger scheme

3.3 Charge measurement

A slow shaper in used in this measurement path. The output of the pre-amplifier will arrive first to a network of resistor and capacitor (RC buffer) in order to perform current-to-voltage conversion. Afterward this signal is sent to a CRRC2 shaper (Slow Shaper) via a voltage buffer. Both of the RC buffer and CRRC2 shaper have adjustable capacitors values that can be used for adjusting the amplitude and peaking time of the resulting signal. Additionally, there are 2 analog memories (SCA with Track/Hold stage) available for sampling the slow shaper waveform. Each of this memory cells can be controlled individually through dedicated input pins (Hold1/Hold2 – pin 78/81 or AC9/AC10). The sampled signal can be either readout with an external ADC (refer to Section 0) or with the internal Wilkinson type ADC embedded in this ASIC.

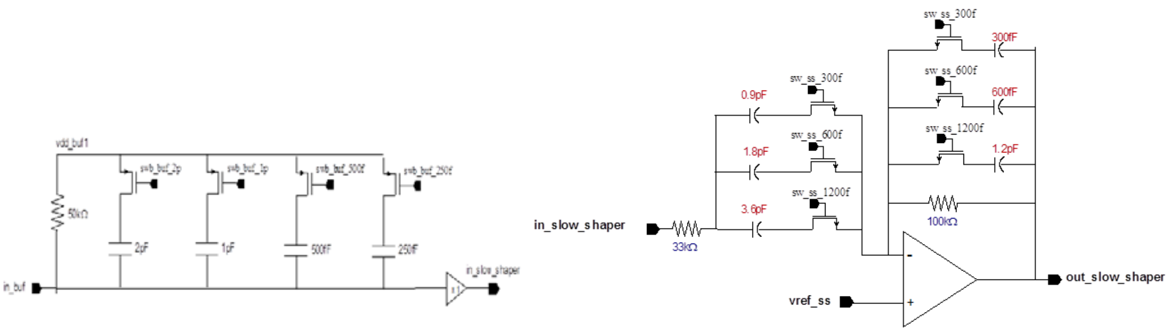


Figure 10 – RC Buffer (left) & Slow Shaper (right)

The feedback and input capacitors of the Slow Shaper can be set through Slow Control parameters (sw_ss_300f, sw_ss_600f & sw_ss_1200f – bit #180,179&178). The available values and the shaper time constant, R*C, are reported in Table 8.

sw_ss_1200f, sw_ss_600f & sw_ss_300f	Input capacitor	R*C (Input R = 33kOhm)	Feedback capacitor	R*C (Feedback R = 100kOhm)
"000"	0	0	0	0
"001"	0.9 pF	30 ns	0.3 pF	30 ns
"010"	1.8 pF	60 ns	0.6 pF	60 ns
"011"	2.7 pF	89 ns	0.9 pF	90 ns
"100"	3.6 pF	119 ns	1.2 pF	120 ns
"101"	4.5 pF	149 ns	1.5 pF	150 ns
"110"	5.4 pF	178 ns	1.8 pF	180 ns
"111"	6.3 pF	208 ns	2.1 pF	210 ns

Table 8 - Slow Shaper feedback/input capacitor values and R*C time constant

The RC buffer in Figure 10 can be configured by setting the value of the capacitor which is in parallel with a 50 kOhm resistor. Basically setting up this capacitor value could change the amplitude and also duration of the signal fed to the Slow Shaper. This capacitor is accessible through Slow Control parameters; swb_buf_2p, swb_buf_1p, swb_buf_500f & swb_buf_250f – bits #182,183,184 & 185. The value of the capacitors and the resulting time constant of this buffer are listed in Table 9.

swb_buf_2p, swb_buf_1p, swb_buf_500f & swb_buf_250f	RC buffer capacitor	Time Constant = R*C (R = 50kOhm)	swb_buf_2p, swb_buf_1p, swb_buf_500f & swb_buf_250f	RC buffer capacitor	Time Constant = R*C (R = 50kOhm)
"0000"	3.75 pF	187.5 ns	"1000"	1.75 pF	87.5 ns
"0001"	3.5 pF	175 ns	"1001"	1.5 pF	75 ns
"0010"	3.25 pF	162.5 ns	"1010"	1.25 pF	62.5 ns
"0011"	3 pF	150 ns	"1011"	1 pF	50 ns
"0100"	2.75 pF	137.5 ns	"1100"	0.75 pF	37.5 ns
"0101"	2.5 pF	125 ns	"1101"	0.5 pF	25 ns
"0110"	2.25 pF	112.5 ns	"1110"	0.25 pF	12.5 ns
"0111"	2 pF	100 ns	"1111"	0	0

Table 9 - RC buffer capacitor values and time constant

The resulting peaking time will depend on the settings applied to the RC buffer and the Slow Shaper feedback capacitors. Measured peaking time for selected RC buffer and Slow Shaper is reported in Table 10.

Peaking Time		Slow Shaper Feedback Capacitor			
		0.3 pF	0.9 pF	1.6 pF	2.1 pF
RC buffer capacitor	0	50 ns	66 ns	76 ns	84 ns
	0.5 pF	54 ns	76 ns	89 ns	95 ns
	3 pF	61 ns	93 ns	122 ns	139 ns
	3.5 pF	62 ns	92 ns	126 ns	142 ns

Table 10 - Slow Shaper peaking time for feedback capacitor vs RC buffer capacitor

3.3.1 SCA Track/Hold mechanism

For charge measurement purpose, either by internal Wilkinson ADC or external ADC, the Track/Hold signal has to be provided from an external source. For each Slow Shaper, there are 2 SCA or analog memories available for storing the Slow Shaper amplitude. These memories will only store the amplitude once "Hold" signal is received via 2 input pads (Hold1/Hold2 – pin 78/81 or AC9/AC10). Unlike the Slow Shaper and SCA which are available for each channel, Hold1 and Hold2 inputs are common to all 64 channels. The following figures will illustrate the usage of these Hold signals.

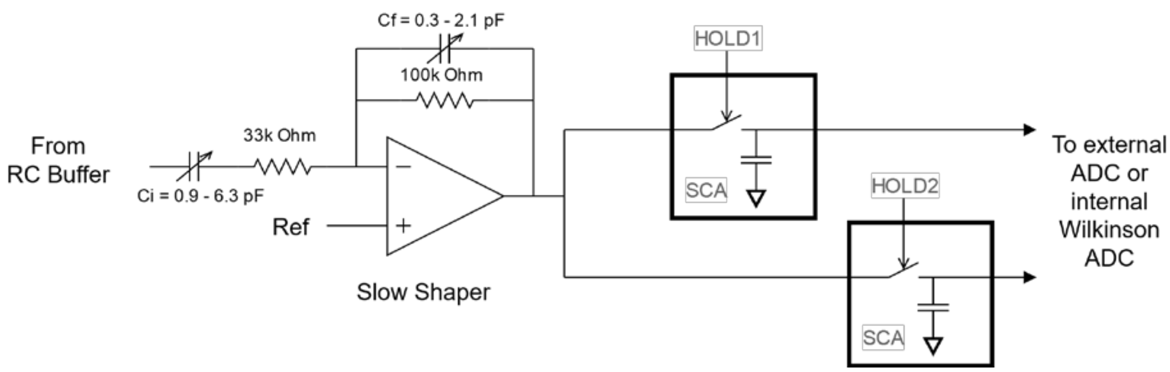


Figure 11 - Slow Shaper SCA block diagram

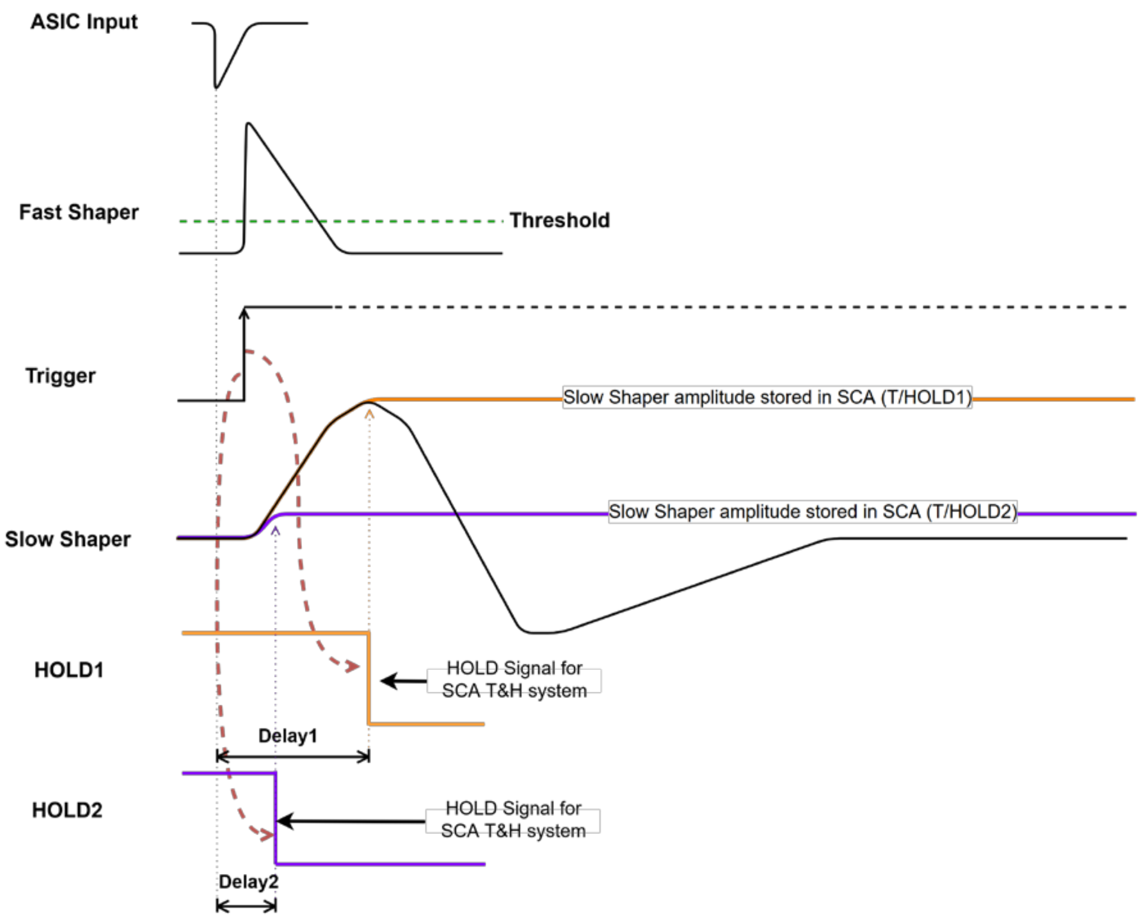


Figure 12 – HOLD1 & HOLD2 input usage for sampling Slow Shaper amplitude via SCA

As depicted in Figure 12, the Hold signals will store the Slow Shaper amplitudes in the corresponding SCA once these signals are at low level. Therefore the arrival of Hold signal is crucial as once this signal goes to low level, the Slow Shaper amplitude will be stored for current condition of this shaper. It is important for user to set the falling edge arrival of the Hold signals which is usually slightly delayed w.r.t to input signal of the detector (Delay1 and Delay2 in Figure 12).

For example, in order to sample the peak of the shaper, user could provide the delay (Delay1 in Figure 12) corresponding the peaking time of the Slow Shaper (refer to Table 10 – delay between input and when shaper start to peak is negligible). On the other hand, if the baseline of Slow Shaper is required, user could simply provide the Hold signal right after the input arrival (Delay2 in Figure 12) or even before the input signal arrival.

Additionally, since the ASIC triggers are available on the output pins, user could use this information to determine the proper delay to be applied for each Hold input.

3.4 Backend and data readout

Analog to Digital conversion is performed by Wilkinson ADC (ramp type conversion) working at 40MHz (system clock). The conversion is performed by measuring the elapsed time between the start of a voltage ramp and its crossing, detected by the comparator, of the signal to be converted. The time measurement is achieved by a Gray counter not started simultaneously with the ramp. Indeed the launching of the ramp is ordered by the start_ADC (pin 116 or AB19) input falling edge signal. The crossing between the ramp and the reference voltage of the slow shaper generates a trigger pulse which becomes the start of the Gray counter. When a comparator triggers, its output is synchronized by system clock in order to memorize the state of the counter which will be the converted data.

The 12-bit Gray counter and the ramp generator are shared between all the channels. The ADC part replicated in each channel can be reduced to a discriminator and memory array is used to copy and memorize the counter state when the discriminator triggers. So the power consumption and the area used can be very small even for high dynamic range.

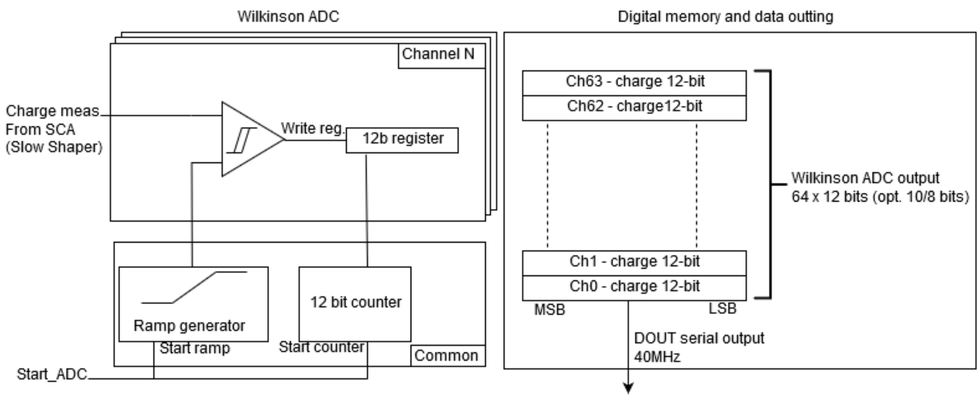
The use of this kind of ADC is limited by its long conversion time. In fact, for an *N* bit conversion, it requires $2^N / Fck$, where *Fck* is the clock period of the counter. For a 12-bit conversion, running at 40 MHz, 102.4µs are required to perform a full conversion. Users could also reduce the conversion time by selecting lower resolution, i.e. 10-bit or 8-bit conversion.

The ramp begins at the start_ADC (pin 116 or AB19) falling edge and the readout of the data starts automatically at the end of the conversion. Data are synchronised with the rising edge of the TransmitOn signal and this signal will stay active until the end of data transmission. The length of the TransmitON signal will depend on the number of bits to be transmitted which is directly related to the chosen ADC resolution. For example, when 12-bit conversion is selected, in total 768 bits covering 64 channels will be transmitted. Given that each bit width is 25 ns (40MHz serial data transmission), total time taken for data transmission and TransmitOn width is exactly 19.2us. Data transmission begins with channel 0 and the first bit will the LSB of the converted data. Then channel order is increased one by one until channel 63. Both of the data and TransmitOn signals are available at pin out_ADC (pin 115 or AC19) and TransmitON (pin 114 or W17) respectively.

Converting the readout data to voltage can be done according this equation:

$$\text{Converted voltage (mV)} = 970\text{ mV} + (\text{data x LSB})$$

LSB value depends on the conversion resolution and can be consulted in Table 11 .



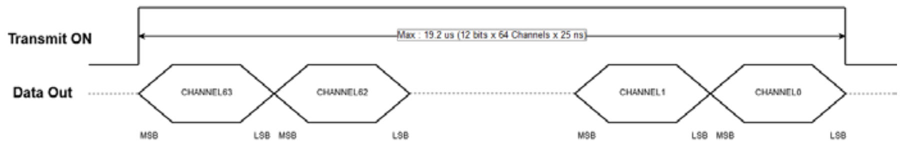


Figure 13 - Wilkinson ADC architecture and data readout scheme

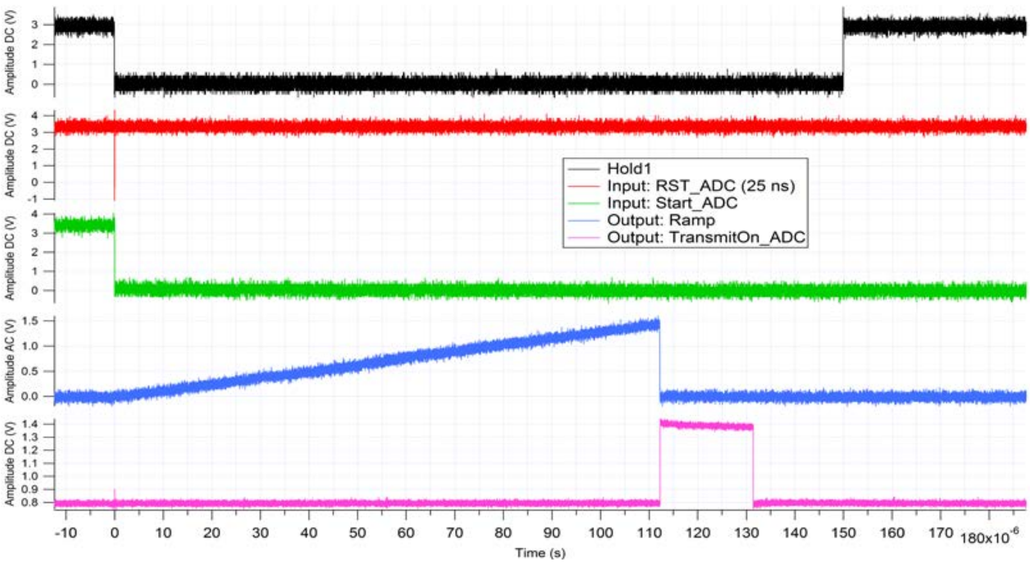


Figure 14 - Example of ADC Wilkinson operation timing diagram

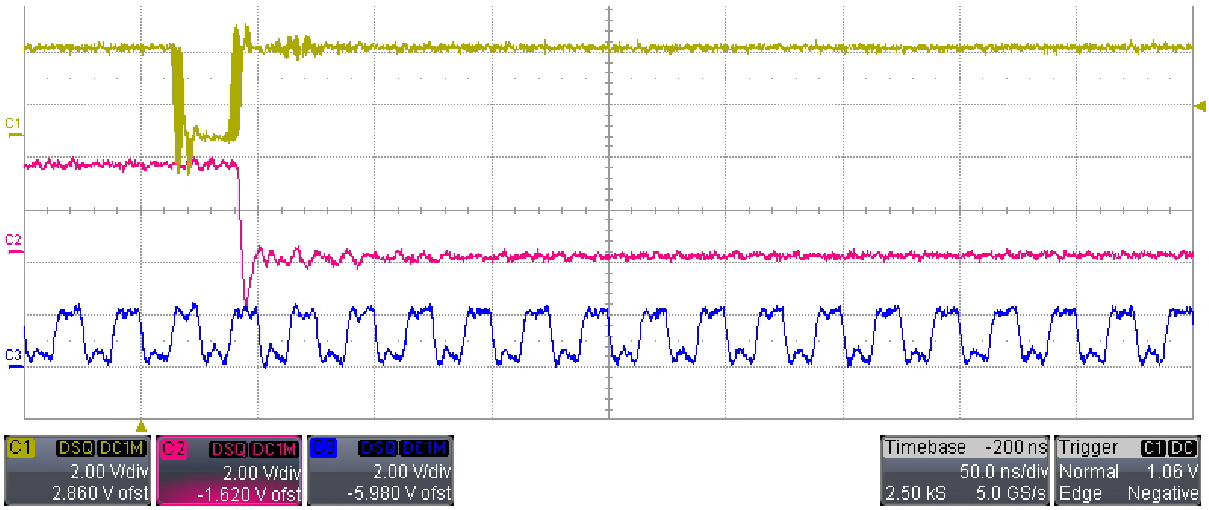


Figure 15 – Recommended timing and pulse width of ADC reset and conversion start wrt 40 MHz system clock. Yellow : ADC Reset (RST_ADC) low level width of 25 ns. Pink : Conversion star t (Start_ADC) falling edge sync to RST_ADC rising edge. Blue: 40 MHz system clock sent to ASIC.

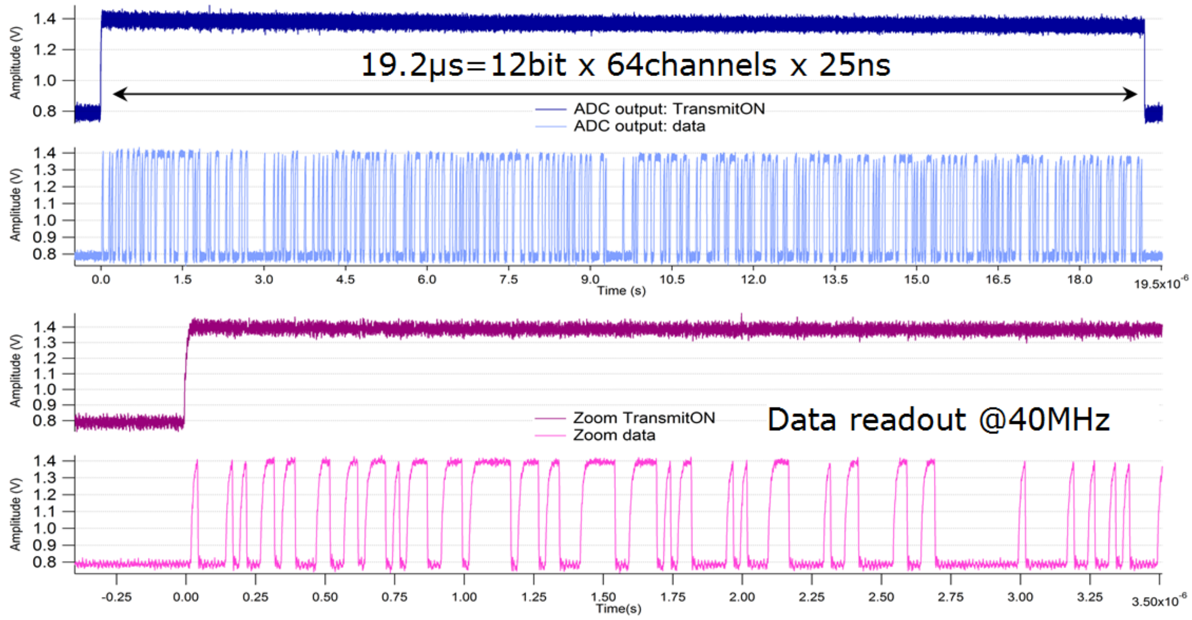


Figure 16 - Data Transmission example timing diagram

ADC Resolution	12bits	10bits	8bits
Max signal conversion time	102µs	25µs	6µs
Data Transmission length	19.2µs	16µs	12.8µs
Total conversion time	121.2µs	41µs	18.8µs
Conversion Rate	8 kEvents/s	24 kEvents/s	53 kEvents/s
LSB	0.257 mV	1.24 mV	5.13 mV

Table 11- Wilkinson ADC max conversion rate and LSB data

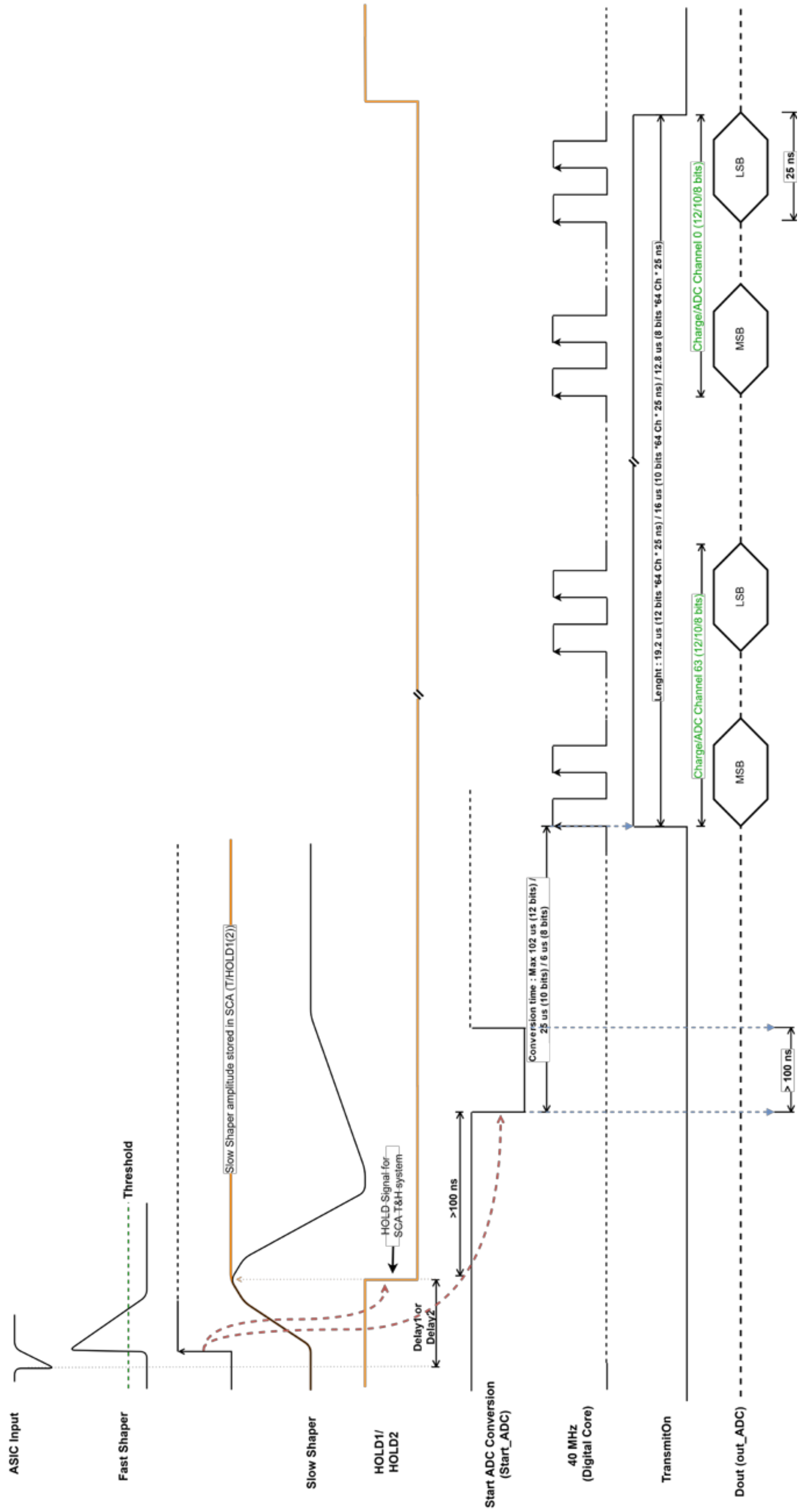


Figure 17 - MAROC3A data conversion and readout timing diagram

4 ASIC programmable parameters

4.1 General description

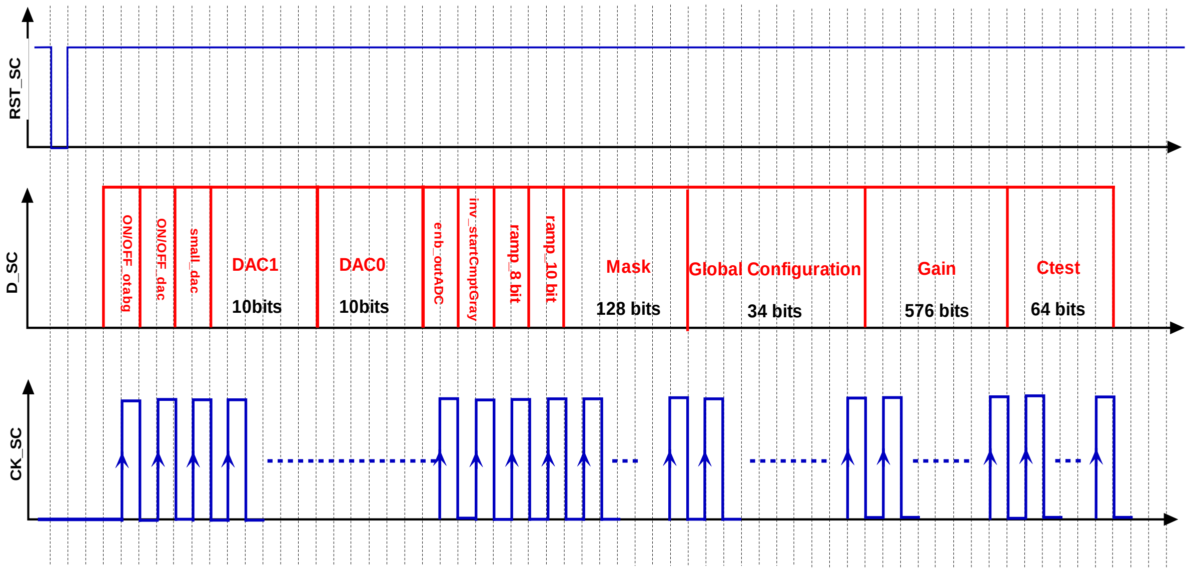


Figure 18 - Slow control timing diagram.

The Slow Control is a shift register composed of *n* flip flops (*n* = 829 flip flops in MAROC3). Data are stored in flip flops on leading edge of the clock. The data are shifted at each clock cycle as shown in Figure 18.

The interface for programming the Slow Control register is the following:

- Reset : RSTn_SC – pin 66 or AB5 → This low-level asynchronous input (> 20 ns) will reset the register to zero.
- Data in: D_SC – pin 63 or AB4 → Slow Control register input. Data is sampled and shifted on the clock rising edge.
- Clock : CK_SC – pin 68 or AC5 → Slow Control clock frequency is recommended to be between 1 MHz to 5 MHz.
- Data out : Qbuf_SC – pin 199 or B15 → Data output is presented on the clock falling edge for MAROC3A and on rising edge for MAROC3. The reason of changing the output to be presented on the clock falling edge is when daisy chaining with other chip, setup/hold violation can be avoided especially if the data is sampled on clock rising edge.

It should be noted that the Reset signal will set the register to '0' and this condition is not a working parameter for the ASIC. Therefore after the reset, user must shift in the bit stream of a known working condition to the ASIC (refer to Table 12 for examples of Slow Control parameters).

Slow Control register parameters :

SC name	SC description	Bit #	Comment	ASIC Operation Mode		
				Analog triggering	Analog charge meas.	Full digital charge/ trigger meas.
ON/OFF_otabg	power pulsing bit for bandgap	0	not active on evaluation board because power pulsing pin is connected to vdd	1	1	1
ON/OFF_dac	power pulsing bit for all DACs	1	not active on evaluation board because power pulsing pin is connected to vdd	1	Not Used	1
small_dac	to decrease the slope of DAC0 for better accuracy	2	'0' : Disable '1' : Enable	User choice	Not Used	1
DAC2[9]	DAC value for the second discri (with the fast shaper FSB2)	3	VTH1 or DAC1 in Table 6	User custom value	Not Used	User custom value
DAC2[8]		4				
...		...				
DAC2[1]		11				
DAC2[0]		12				
DAC1[9]	DAC value for the first discri (with the fast shaper FSB1 or FSU)	13	VTH0 or DAC0 in Table 6	User custom value	Not Used	User custom value
DAC1[8]		14				
...		...				
DAC1[1]		21				
DAC1[0]		22				
enb_outADC	Wilkinson ADC parameter: enable data output	23	'0' enable , '1' disable	1	1	0
inv_startCmptGray	Wilkinson ADC parameter: the start ADC signal polarity switch	24	0' enable , '1' disable	1	1	0
ramp_8bit	Wilkinson ADC parameter: ramp slope adjustment for 8-bit conversion	25	'1' for 8-bit ADC conversion. '0' for 12-bit ADC conversion.	Not used	Not used	0
ramp_10bit	Wilkinson ADC parameter: ramp slope adjustment for 10-bit conversion	26	'1' for 10-bit ADC conversion. '0' for 12-bit ADC conversion.	Not used	Not used	0
mask_OR2_ch63	mask the second discri output of ch63 (FSB2 to generate the trigger)	27	Mask2 for D2 discriminator in Figure 9: '1': disable trigger output '0': enable trigger output	0	Not used	0
mask_OR1_ch63	mask the first discri output of ch63 (FSB1 or FSU	28	Mask1 for D1 discriminator in Figure 9: '1': disable trigger output	0	Not used	0

	to generate the trigger)		'0': enable trigger output			
mask _OR2_ch62	mask the second discri output of ch62 (FSB2 to generate the trigger)	29	Mask2 for D2 discriminator in Figure 9: '1': disable trigger output '0': enable trigger output	0	Not used	0
mask_OR1_ch62	mask the first discri output of ch62 (FSB1 or FSU to generate the trigger)	30	Mask1 for D1 discriminator in Figure 9: '1': disable trigger output '0': enable trigger output	0	Not used	0
...		...				
mask_OR2_ch1	mask the second discri output of ch1 (FSB2 to generate the trigger)	151	Mask2 for D2 discriminator in Figure 9: '1': disable trigger output '0': enable trigger output	0	Not used	0
mask_OR1_ch1	mask the first discri output of ch1 (FSB1 or FSU to generate the trigger)	152	Mask1 for D1 discriminator in Figure 9: '1': disable trigger output '0': enable trigger output	0	Not used	0
mask _OR2_ch0	mask the second discri output of ch0 (FSB2 to generate the trigger)	153	Mask2 for D2 discriminator in Figure 9: '1': disable trigger output '0': enable trigger output	0	Not used	0
mask_OR1_ch0	mask the first discri output of ch0 (FSB1 or FSU to generate the trigger)	154	Mask1 for D1 discriminator in Figure 9: '1': disable trigger output '0': enable trigger output	0	Not used	0
cmd_CK_mux		155	Unused & mandatory set to '0'	0	0	0
d1_d2	trigger output choice	156	Refer to Figure 9 and Section 3.2.1 : '0': trigger from D1 discriminator '1': trigger from D2 discriminator	User choice	Not used	User Choice
inv_discriADC	Wilkinson ADC discriminator output inversion	157	Should be OFF '0' : active High '1': active Low	Not used	Not used	0
polar_discri	polarity of trigger output	158	'0' : active High '1': active Low	0	Not used	0
Enb_tristate	enable all trigger tri-state output buffers	159	'1' :enable '0': disable	1	0	1
valid_dc_fsb2	enable FSB2 DC measurements	160	'1' :enable '0': disable	0	0	0
sw_fsb2_50f	Feedback capacitor for FSB2	161	Refer to Table 2 for Half Bipolar Fast Shaper feedback capacitor value selection	1	Not Used	1
sw_fsb2_100f	Feedback	162		1	Not	1

	capacitor for FSB2				Used	
sw_fsb2_100k	Feedback resistor for FSB2	163	Refer to Table 2 for Half Bipolar Fast Shaper feedback resistor value selection	0	Not Used	0
sw_fsb2_50k	Feedback resistor for FSB2	164		0	Not Used	0
valid_dc_fs	enable FSB and FSU DC measurements	165		0	0	0
cmd_fsb_fsu	Choice between FSB1 or FSU for the first discri input (with DAC0)	166	cmd_fsb_fsu='1'-> FSU ; cmd_fsb_fsu='0'-> FSB	User Choice	Not used	User Choice
sw_fsb1_50f	Feedback capacitor for FSB1	167	Refer to Table 2 for Bipolar Fast Shaper feedback capacitor value selection	1	Not Used	1
sw_fsb1_100f	Feedback capacitor for FSB1	168		1	Not Used	1
sw_fsb1_100k	Feedback resistor for FSB1	169	Refer to Table 2 for Bipolar Fast Shaper feedback resistor value selection	0	Not Used	0
sw_fsb1_50k	Feedback resistor for FSB1	170		0	Not Used	0
sw_fsu_100k	Feedback resistor for FSU	171	Refer to Table 4 for Unipolar Fat Shaper feedback resistor value selection	0	Not Used	0
sw_fsu_50k	Feedback resistor for FSU	172		0	Not Used	0
sw_fsu_25k	Feedback resistor for FSU	173		0	Not Used	0
sw_fsu_40f	Feedback capacitor for FSU	174	Refer to Table 4 for Unipolar Fast Shaper feedback capacitor value selection	1	Not Used	1
sw_fsu_20f	Feedback capacitor for FSU	175		1	Not Used	1
H1H2_choice	ADC wilkinson: choice between the first or the second track and hold for the input of the ADC	176	The selection of the internal SCAs : '0' : SCA2 '1' : SCA1	Not used	User choice	User choice
EN_ADC	ADC wilkinson: enable ADC conversion inside the asic	177	Should be ON to make a conversion '1': Enable conversion '0':Disable conversion	0	0	1
sw_ss_1200f	Feedback capacitor for Slow Shaper	178	Refer to Table 8 for Slow Shaper feedback capacitor value selection	Not Used	1	1
sw_ss_600f	Feedback capacitor for Slow Shaper	179		Not Used	1	1
sw_ss_300f	Feedback capacitor for Slow Shaper	180		Not Used	1	1
ON/OFF_ss	Power supply of	181	'0' : disable Slow Shaper	0	1	1

	Slow Shaper		'1': enable Slow Shaper			
swb_buf_2p	capacitor for the buffer before the slow shaper	182	Refer to Table 9 for RC buffer capacitor value selection	Not Used	1	1
swb_buf_1p	capacitor for the buffer before the slow shaper	183		Not Used	1	1
swb_buf_500f	capacitor for the buffer before the slow shaper	184		Not Used	1	1
swb_buf_250f	capacitor for the buffer before the slow shaper	185		Not Used	1	1
cmd_fsb	enable signal at the FSB inputs	186	Should be ON ('1') if FSB1 or FSB2 is used for triggering	User choice	Not Used	User Choice
cmd_ss	enable signal at the SS inputs	187	Should be ON ('1') if internal charge measurement is used	Not Used	1	1
cmd_fsu	enable signal at the FSU inputs	188	Should be ON ('1') if FSU is used for triggering	User choice	Not Used	User choice
cmd_SUM63	enable signal to do sum	189		0	0	0
GAIN63[7]	preamplifier gain value channel 63	190	Refer to Section 3.1 for pre-amplifier gain setting. Recommended Gain = 1 - ("1000 0000").	1	1	1
GAIN63[6]		191		0	0	0
GAIN63[5]		192		0	0	0
GAIN63[4]		193		0	0	0
GAIN63[3]		194		0	0	0
GAIN63[2]		195		0	0	0
GAIN63[1]		196		0	0	0
GAIN63[0]		197		0	0	0
cmd_SUM62	enable signal to do sum	198		0	0	0
GAIN62[7]	preamplifier gain value channel 63	199	Refer to Section 3.1 for pre-amplifier gain setting. Recommended Gain = 1 - ("1000 0000").	1	1	1
GAIN62[6]		200		0	0	0
GAIN62[5]		201		0	0	0
GAIN62[4]		202		0	0	0
GAIN62[3]		203		0	0	0
GAIN62[2]		204		0	0	0
GAIN62[1]		205		0	0	0
GAIN62[0]		206		0	0	0
...		...				
GAIN0[7]	preamplifier gain value channel 0	757	Refer to Section 3.1 for pre-amplifier gain setting. Recommended Gain = 1 - ("1000 0000").	1	1	1
GAIN0[6]		758		0	0	0
GAIN0[5]		759		0	0	0
GAIN0[4]		760		0	0	0
GAIN0[3]		761		0	0	0
GAIN0[2]		762		0	0	0
GAIN0[1]		763		0	0	0
GAIN0[0]		764		0	0	0
Ctest_ch63	enable signal in	765	Ctest : internal charge injection	0	0	0

	Ctest input		capacitor (2pF)			
Ctest_ch62	enable signal in Ctest input	766	Ctest : internal charge injection capacitor (2pF)	0	0	0
Ctest_ch61	enable signal in Ctest input	767	Ctest : internal charge injection capacitor (2pF)	0	0	0
…	enable signal in Ctest input	….	Ctest : internal charge injection capacitor (2pF)	0	0	0
Ctest_ch2	enable signal in Ctest input	826	Ctest : internal charge injection capacitor (2pF)	0	0	0
Ctest_ch1	enable signal in Ctest input	827	Ctest : internal charge injection capacitor (2pF)	0	0	0
Ctest_ch0	enable signal in Ctest input	828	Ctest : internal charge injection capacitor (2pF)	0	0	0

Table 12 – Slow control register parameters

4.2 Read register parameters

A read register is integrated for debugging and also reading out analog multiplexer for charge measurement. The 2 analog outputs are available on out_fs (pin 201 or B14) for fast shaper waveforms and on out_q (pin 215 or A10) for Slow Shaper waveform.

This read register works similarly as the SC registers described previously except for its data input. It is controlled by CK_R (pin 78 or AB9), RSTb_R (pin 80 or AB10) and D_R (pin 82 or AB11). The probe shift register composed of *128* flip flops. It should be noted that the period of register clock, CK_R, is mostly limited by the analog multiplexer buffer settling time. Therefore it is preferable that CK_R period to be longer than 200 ns.

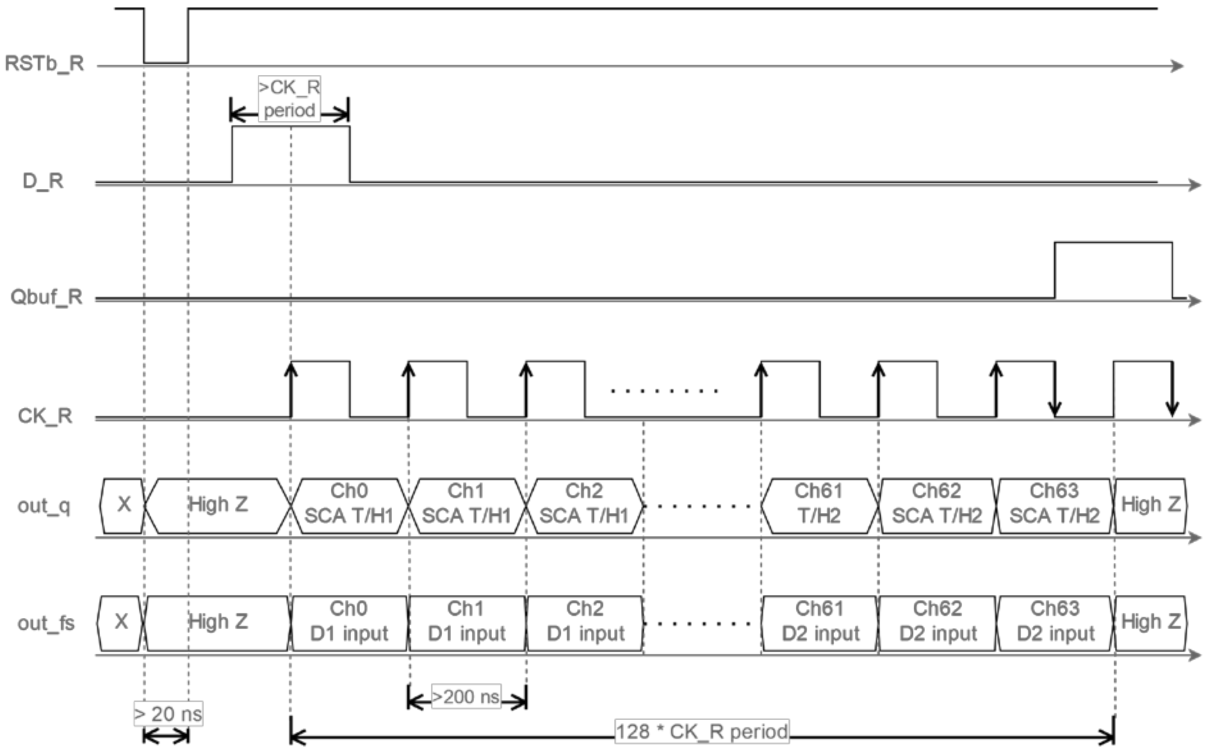


Figure 19 – Read register timing diagram.

Signal name	Probe	Comments	Probe outputs	Bit #
Slow Shaper output	128	Multiplexed output of the 2x64 SCA of Slow Shaper (Section 3.3)	Analog (out_q - pin 215 or A10)	0-127
Fast Shaper Output	128	Multiplexed output of the Fast Shapers at the input of D1 and D2 discriminators (Section 3.2)	Analog (out_fs - pin 201 or B14)	0-127

Table 13 – Read register parameters

5 ASIC I/Os connections

5.1 Input connection

The MAPMT anodes can be connected directly to ASIC as illustrated in Figure 20 and no external component is required for detector connection. The inputs (in<0..63>) are located on various locations of the west side of the QFP and BGA (refer to section 8.1 and 8.2) packages of this ASIC.

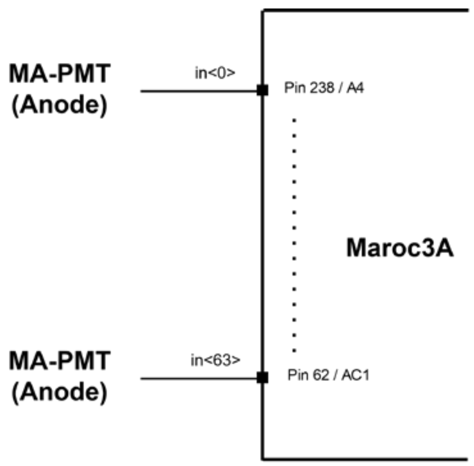


Figure 20 - Maroc3A inputs connection

5.2 Backend connection

The 64 trigger outputs, Out <0:63>, are outputted through an internal output buffer whose external VH (pin 190 or E12-14) and VL (pin 187 or E15-17) supplies must be set outside the chip. No external component is necessary.

The OR_1 (pin 191 or B16) and OR_2 (pin 192 or B17) signal is an analogue OR of the 64 discriminator outputs. OR_1 is an OR of the 64 first trigger (connected to Unipolar Fast shaper or Bipolar Fast Shaper). OR_2 is an OR of the 64 second trigger (connected Half Bipolar Fast Shaper). Trigger outputs and OR outputs connections are shown in Figure 21.

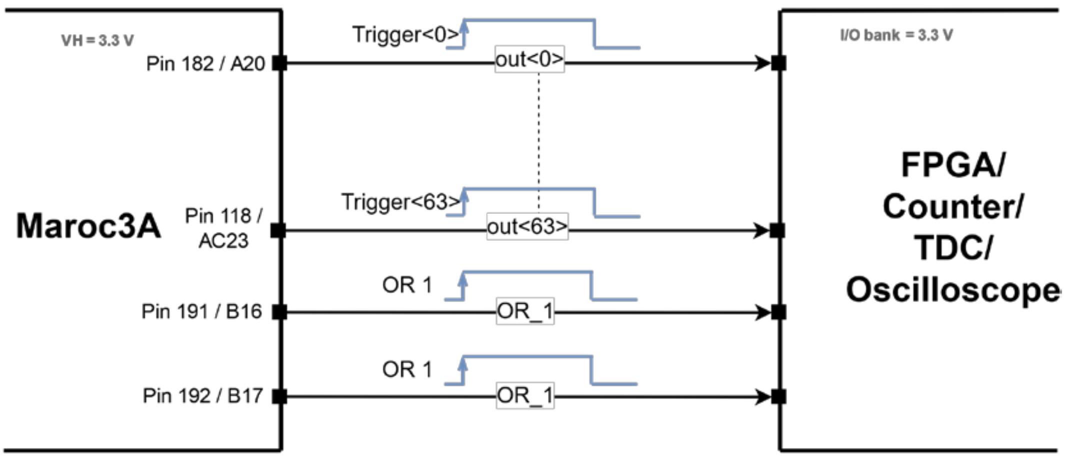


Figure 21 - Maroc3A Trigger and OR outputs connection

The charge measurement is coded internally on 8bits, 10 bits or 12bits depending of the Slow Control parameter. These coded data, out_ADC, are available on pin 115 or AC19. They are outputted through an internal VH/VL output buffer.

During the transmission of the coded data, a TransmitOn signal is generated by the chip. This signal is available on pin 114 or W17. It is also buffered internally by VH/VL buffer.

Additionally other control signals are required for the internal ADC used in charge measurement : ADC Reset (Rstn_ADC, pin 184 or A20 – LVCMOS), Start Conversion (start_ADC, pin 116 or AB19 – LVCMOS), System Clock – 40 MHz (CK_40M &CKb_40M, pin 188 & 86 or A18&19 – LVDS).

The interface for the digital readout is shown in Figure 22. Refer to Section 3.4 for information concerning the backend and digital readout.

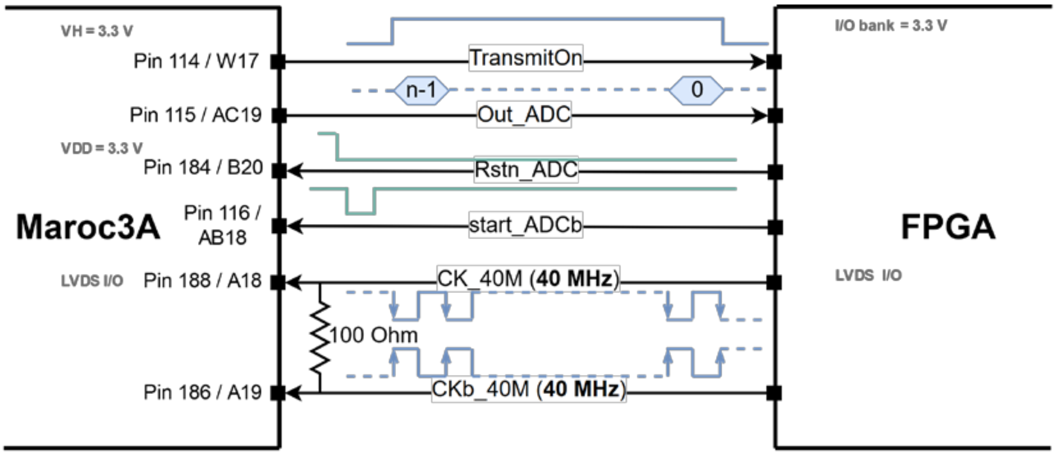


Figure 22 - Maroc3A digital backend connection

The interface for analog Read register (Section 4.2) is illustrated in Figure 23. Multiplexed analog outputs are available at out_fs (pin 201 or B14) and out_q (pin 215 or A10). Depending on the read register value, the output of each fast shaper and track hold can be seen and checked for debug or measurement purpose.

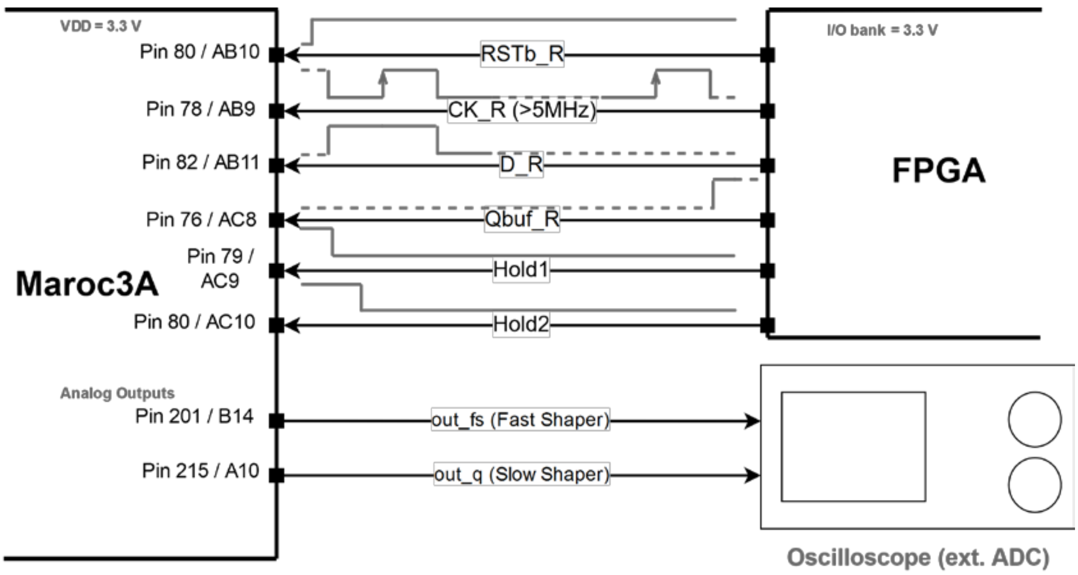


Figure 23 - Maroc3A Read register interface connection

The interface for accessing the Slow Control register (Section 4.1) for configuring the ASIC is illustrated in Figure 24.

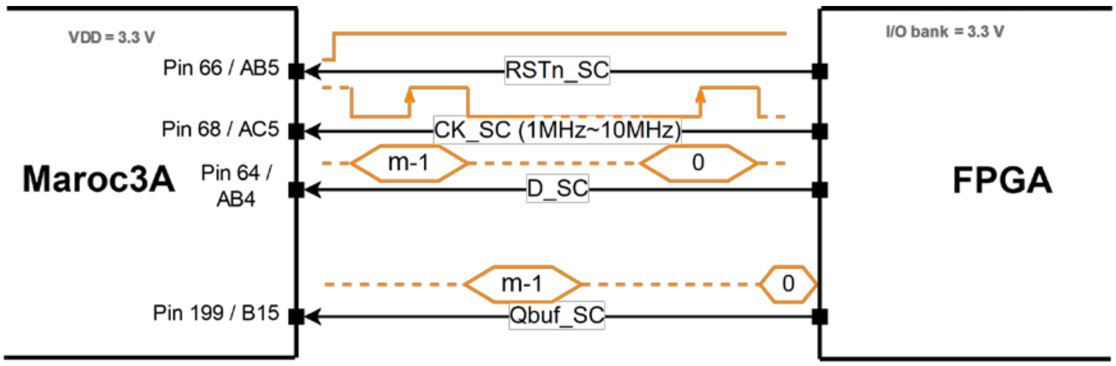


Figure 24 - Maroc3A Slow Control register interface connection.

5.3 Supplies, references, biases

As shown in Section 8.1 describing the pinout of the ASIC in QFP packaging, there are specific power supplies for each block, noted vdd_cellname. The power supplies are separated inside the chip to avoid couplings. However, all the power supplies can be gathered and connected to a common vdd=3.3V (decoupled with 100nF – ideally to each pin) except for the power supplies of the digital blocks vddd and vddd2 which can be connected together to a specific vddd=3.3V (with a 100nF decoupling capacitor – ideally to each pin).

The power supply VH can be set to 1.8V up to 3.3V. VL can be set to ground. Both of these pins are used for powering the trigger, OR and data outputs.

As for the ground pins (gnd_cell) and vss (substrate), they can be all connected to the general ground of the board.

The bias voltages (ib_cell) and reference voltages are made internally and are available on pins (Table 15). No external component is necessary on these points.

For TFBGA package, the power supplies have been regrouped at package level, thus it is directly separated in to 3 main domains : VDDA, VDDD and VH. These power supplies has to be separated and decoupled properly (e.g. 100nF at multiple power supply pins). On the other hand, there are only VSS pins for grounding and VL pins which are also recommended to be connected to the ground. Refer to Figure 25 for power supply strategies for both packages type.

power pin name	Pin number	current (mA)		power pin name	Pin number	current (mA)
vdd_w	83	2.4		vdd_FSU2	204	5.2
vdd_DAC	87	0.65 (dac max) to 1.92 (dac min)		vdd_FSB	210	8.3
vdd_FSU1	90	1,4		vdd_SS	221	8
vdd_wilk	100	4.6		vdd_buf1	223	0.6
vdd_discri	105	3,6		vdd_OTAQ	225	5
vddd2	113	7.1		vdd_pa	233	5.4
vddd	185	0,8		vdd_pad	236	0
vdd_discriADC	193	7.6				

Table 14 – QFP 240 package power pin current draw

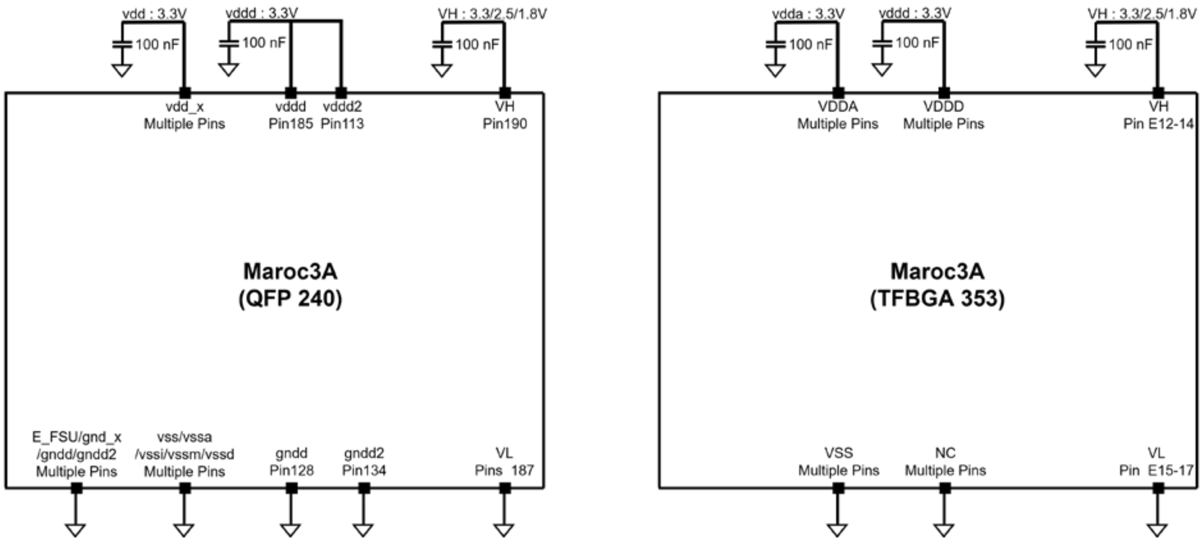


Figure 25 - Power supply connections for QFP (left) and TFBGA (right) packages

6 ASIC performance

6.1 10-bit DACs for Trigger threshold

The linearity of the two DACs (VTH0(DAC0) and VTH1(DAC1)) for setting the trigger threshold have been measured and reported in Figure 26. Settings concerning the DACs configuration are described in Section 3.2.1.

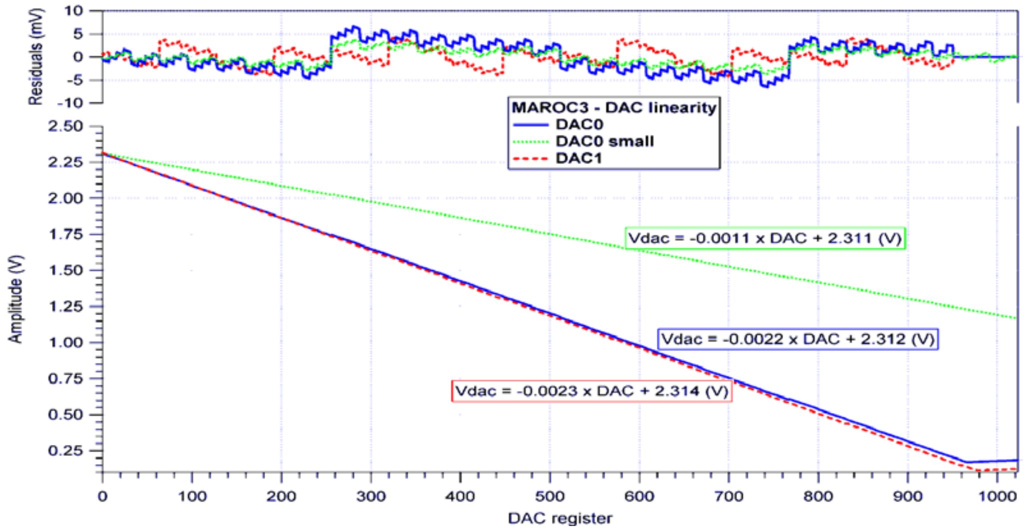


Figure 26 – Trigger threshold linearity measurements

6.2 Trigger measurements

The triggering efficiency versus threshold is measured for Bipolar Fast Shaper (Figure 27) and Unipolar Fast Shaper (Figure 28). The injected charge is around 160 fC (1 photoelecton).

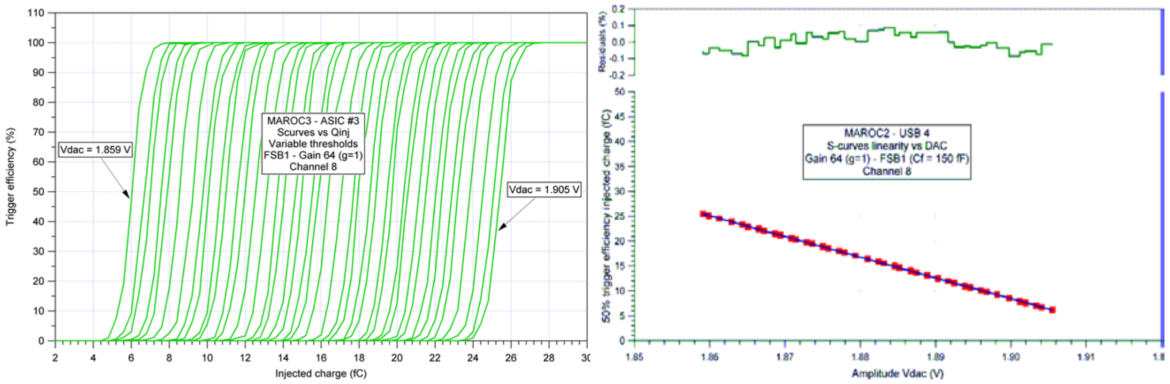


Figure 27 – Left: Bipolar Fast Shaper trigger linearity vs input charge. Right : Linearity plot of triggering efficiency at 50% vs input charge. Slope (inverse) = 2.4V/pC.

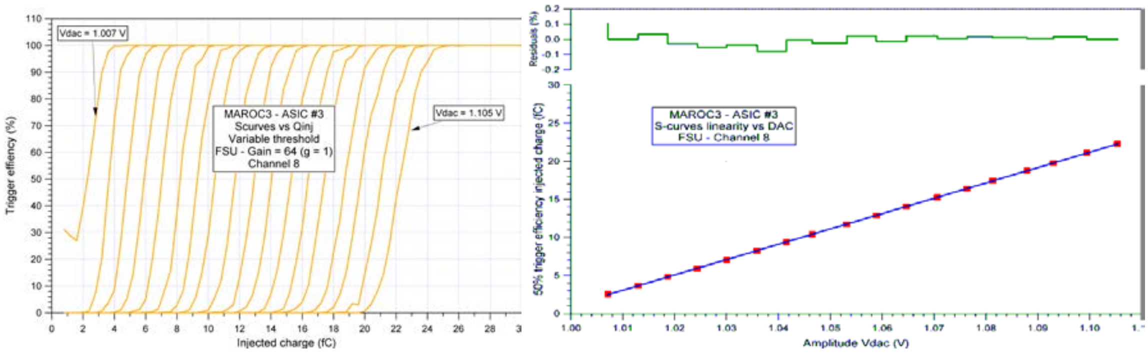


Figure 28– Left: Unipolar Fast Shaper trigger linearity vs input charge. Right : Linearity plot of triggering efficiency at 50% vs input charge. Slope (inverse) = 4.4v/pC.

6.3 Trigger measurement with pre-amplifier gain adjustment

The trigger efficiency with gain dispersion correction is reported in Figure 29. On left side of the figure, trigger efficiency before (Top-Left figure) and after the dispersion correction (Bottom-Left figure). On Top-Right side of the figure, the 50% triggering efficiency is reported for each channel (with and without dispersion correction). Meanwhile on the Bottom-Right figure, gain correction applied to the pre-amplifier is reported for each channel.

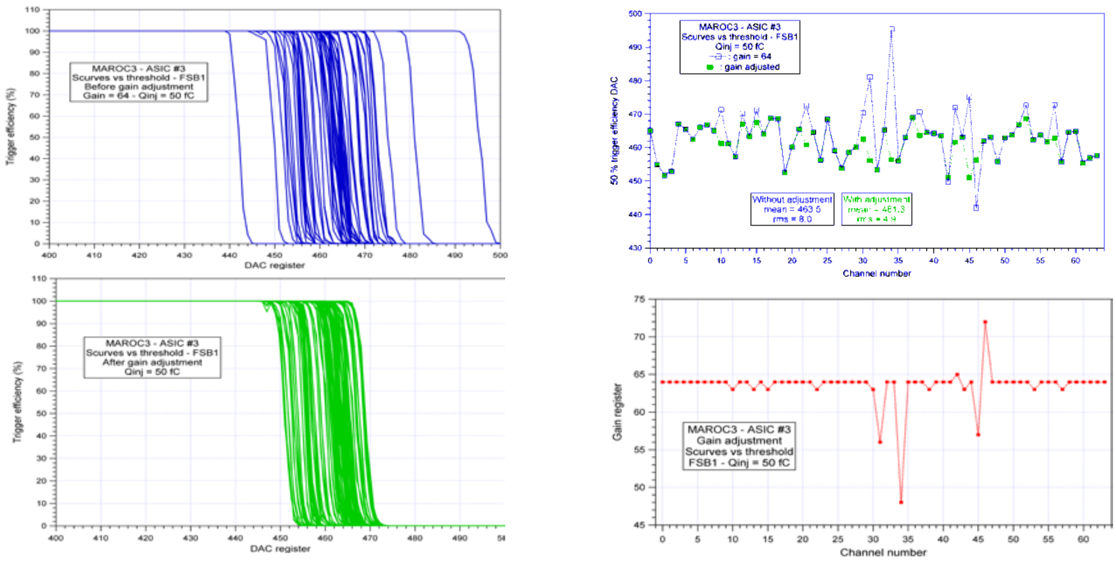


Figure 29 - Pre-amplifier gain adjustment for Bipolar Fast Shaper

6.4 Trigger jitter and time walk

Jitter and time walk of the ASIC trigger output versus injected input charge were measured with 50 fC (1/3 photoelectron). The results are reported in Figure 30.

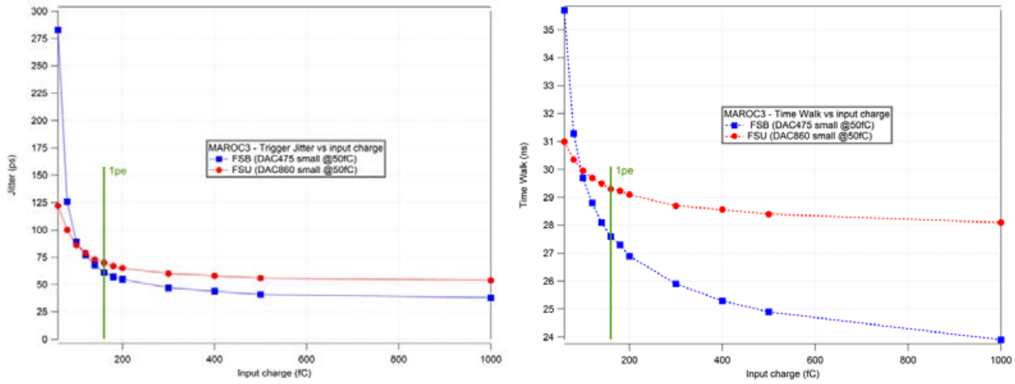
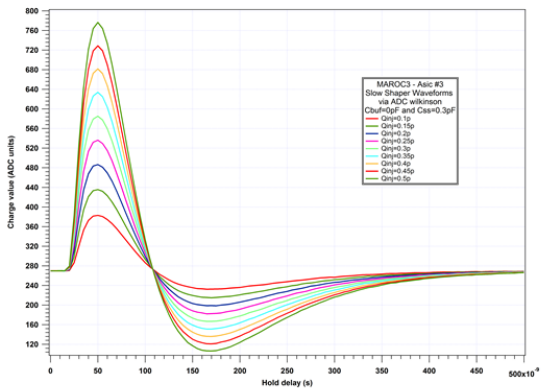


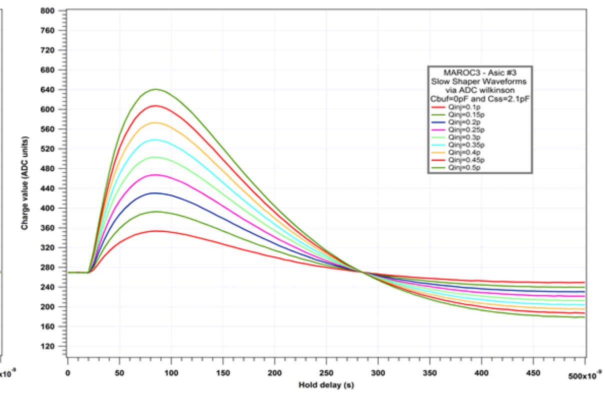
Figure 30 - Timing measurements for Bipolar Fast Shaper and Unipolar Fast Shaper. Left : Jitter. Right: Timewalk.

6.5 Charge measurements

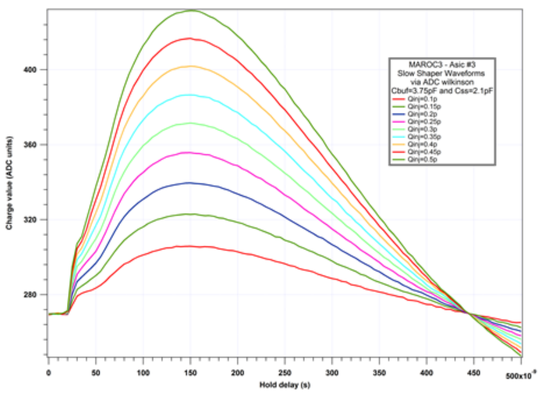
A scan of the hold delay at few input voltage amplitude has been performed. The data converted as function of hold delay have been plotted for 3 shaping configurations. All the measurements are performed using internal Wilkinson ADC.



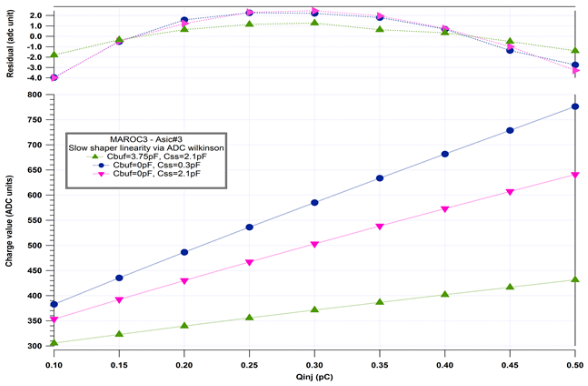
(a)



(b)



(c)



(d)

Figure 31 – (a, b, & c) Slow Shaper waveform versus various hold delay and input charge. (d) Slow Shaper linearity at different shaping time.

7 Result summary

		MAROC3A
	Power Consumption (3.3V)	220mW (➔ 3.5mW/channel)
Detector inputs	Channel	64
	Polarity	negative
	Input impedance	about 50-60 Ω
Backend outputs	Triggers	64 triggers (VH=3.3/2.5/1.8V and VL=0V)
	Charge (ADC)	1 analog multiplex output 1 digital charge (12, 10 or 8 bits)
Pre-Amplifier	Gain variable	8 bits (0 to ~4)
Bipolar Fast Shaper	Gain	371 mV/p.e (2.32V/pC)
	Noise	1.6mV
	Min charge	5fC
	Jitter@160fC (for DAC@50fC)	61ps
Unipolar Fast Shaper	Gain	720 mV/p.e (4.5V/pC)
	Noise	2.4mV
	Min charge	3fC
	Jitter@160fC (for DAC@50fC)	70ps
Slow shaper	Gain	55mV/pC (gain64) – shaping=160ns
	Noise	0.58mV

8 ASIC pinout

MAROC3 is packaged in QFP 240 and also TF-BGA 353 packages.

8.1 QFP 240 package

8.1.1 Pin type description

Pin#	Pin name	Description	Connection
1	in<3>	Analog. Input	Input
29	in<31>	Analog. Input	Input
30	gnd_pa	Analogue (Pre-Amplifier) Ground	GND
31	in<32>	Analog. Input	Input
60	in<61>	Analog. Input	Input
61	in<62>	Analog. Input	Input
62	in<63>	Analog. Input	Input
63	gnd_pa	Analogue (Pre-Amplifier) Ground	GND
64	D_SC	Slow Control Register Input	Input
65	vssa	Inputs Bulk	GND
66	RSTn_SC	Selected Register Reset	Input
67	vdd_pa	Analogue (Pre-Amplifier) Power	VDD
68	CK_SC	Slow Control Register Clock	Input
69	vgain_pa	Pre Amps bias voltage	NC
70	ibi_ss	Slow shaper input bias current	NC
71	vcasc_pmos	Pre Amps bias voltage	NC
72	ibo_ss	Slow shaper output bias current	NC
73	gnd_nmos	Analogue (Pre-Amplifier) Ground	GND
74	ibi_buf	Buffer bias current	NC
75	vref_ss	Slow shaper reference voltage	NC
76	Qbuf_R	Multiplexeur Register Output	Output
77	gnd_w	ADC Ground	GND
78	CK_R	Multiplexeur Register Clock	Input
79	Hold1	Hold Signal	Input
80	RSTb_R	Multiplexeur Register Reset	Input
81	Hold2	Hold Signal	Input
82	D_R		Input
83	vdd_w	ADC power	VDD
84	ibo_dac	10-bit dual DAC output bias current	NC
85	gnd_dac	10-bit dual DAC ground	GND
86	iref_dac	10-bit dual DAC bias current	Bias: Rx to VDD and Rx to gnd if needed or NC
87	vdd_dac	10-bit dual DAC power	VDD
	ibi_dac		
88	vref_dac	10-bit dual DAC reference voltage	NC
89	vbi_tz	FSU input bias current	Bias: Rx to VDD and Rx to gnd if needed or NC
90	vdd_fsu1	FSU power	VDD
91	G_diode	FSU bias voltage	NC

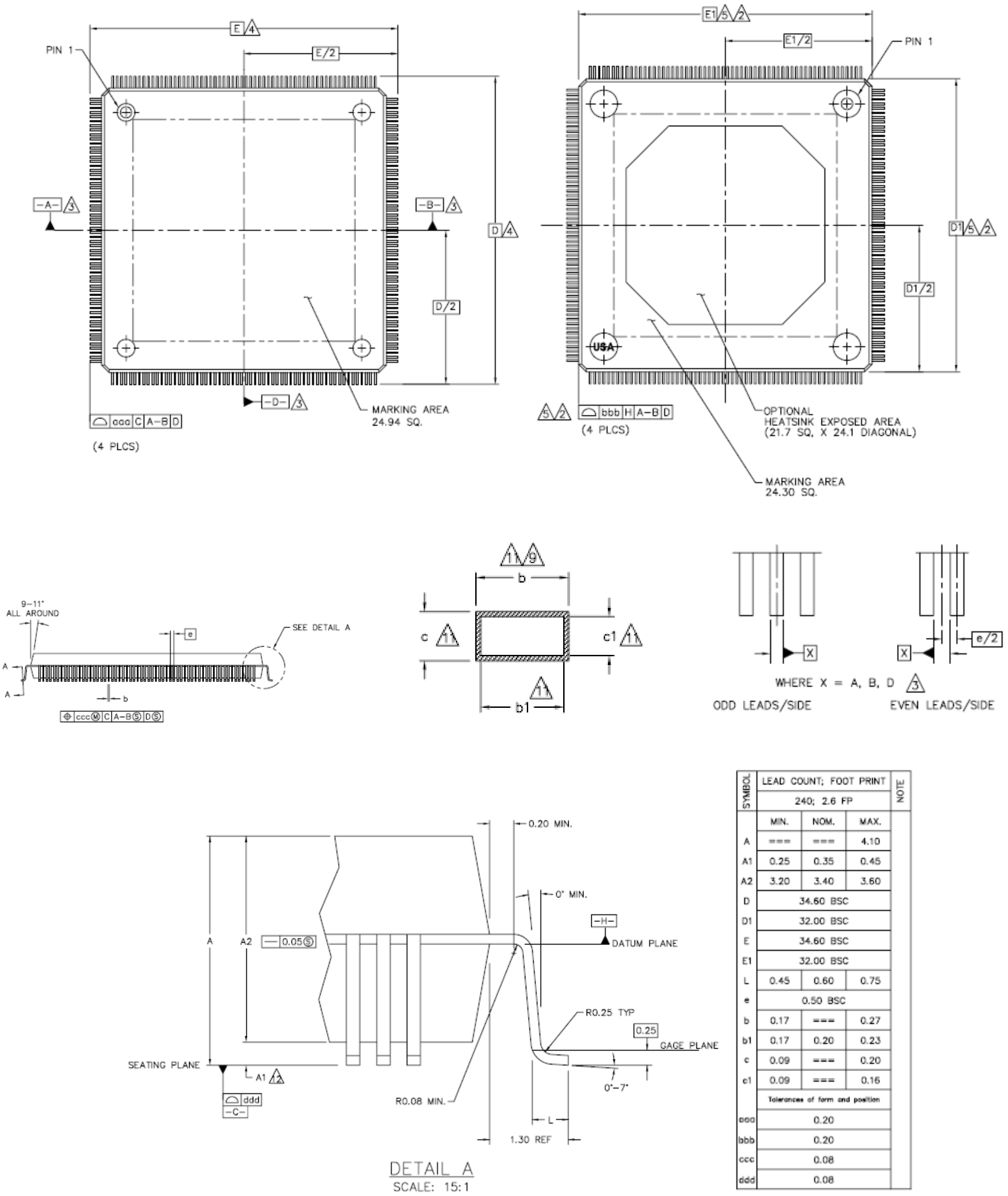
92	E_fsu	FSU ground	GND
93	vbo_tz	FSU output bias current	Bias: Rx to VDD and Rx to gnd if needed or NC
94	vcasc_fsu	FSU bias voltage	NC
95	vslope	ADC Ramp bias voltage	Rx to VDD and Rx to gnd if needed or NC
96	vref_fsu	FSU reference voltage	NC
97	ramp	Ramp output	Output: Pin test
98	gnd_wilk	ADC ground	GND
99	vref_ramp	ADC ramp reference voltage	Rx to VDD and Rx to gnd if needed or NC
100	vdd_wilk	ADC power	VDD
101	ib_integ	ADC bias current	NC
102	vssa	Inputs Bulk	GND
103	vssm	Inputs Bulk	GND
104	vbi_discri	Discriminator input stage bias current	NC
105	vdd_discri	Mixed (Discriminator) Power Supply	VDD
106	vbm_discri	Discriminator middle stage bias current	NC
107	vdd_discriAD C	ADC (Discriminator) Power Supply	VDD
108	vbo_discri	Discriminator output stage bias current	Bias: Rx to VDD and Rx to gnd if needed or NC
109	gnd_discri	Analogue (Discriminator) Ground	GND
110	PWR_ON	should be set to vdd value (3.5V)	Input
111	vssd	Digital part Bulk	GND
112	gndd	Digital (LVDS receivers & Digital) Ground	GND
113	vddd2	Digital (LVDS receivers & digita) Power	VDDD
114	TransmitOn	ADC Active data readout	Output
115	out_ADC	ADC serial data ouput	Output
116	start_ADC	ADC start input	Input
117	vbi_discriADC	Rx to vdda and Rx to gnd if needed	Rx to vdda and Rx to gnd if needed or NC
118	out<63>	Trigger output	Output
119	out<62>	Trigger output	Output
120	out<61>	Trigger output	Output
121	out<60>	Trigger output	Output
150	vssd	Digital part Bulk	GND
180	out<2>	Trigger output	Output
181	out<1>	Trigger output	Output
182	out<0>	Trigger output	Output
183	gndd	Digital (LVDS receivers & Digital) Ground	GND
184	RST_ADC	ADC reset input	Input
185	vddd	Digital (LVDS receivers & digital) Power	VDDD
186	CKb_40M	ADC: 40MHz Clock	Input
187	VL	Low value of the trigger voltage and ADC outputs	Input: Low value of the

		(700mV,100nF to gnd)	trigger voltage (700mV,100nF to gnd) or the ground
188	CK_40M	ADC : 40MHz Clock	Input
189	vssd	Digital part Bulk	GND
190	VH	High value of the trigger voltage and ADC outputs(1.5V,100nF to gnd)	Input: High value of the trigger voltage (1.5V,100nF to gnd)
191	OR_1	OR of the first discriminators	Pin test
192	OR_2	OR of the second discriminators	Pin test
193	vdd_discriADC	ADC (Discriminator) Power Supply	VDD
194	vth1	10-bit dual DAC output 1	Output: Pin test
195	gnd_discri	The same signal, only the name is changed	GND
196	vth0	10-bit dual DAC output 0	Output: Pin test
197	vssm	Bulk inputs	GND
198	vss		GND
199	Qbuf_SC	Slow control register output	Output
200	v_bg	internal bandgap (value 2,5V) ouput	internal bandgap (value 2,5V): only pin test
201	out_fs	Fast Shapers Output	Output pin test: a buffer should be added
202	gnd_fsu	FSU ground	GND
203	vb_otafsu	FSU bias voltage	NC
204	vdd_fsu2	FSu power	VDD
205	vbo_fsb	FSB output bias current	NC
206	gnd_fsb1	FSB ground	GND
207	vbi_fsb	FSB input bias current	NC
208	vref_fsb	FSB reference voltage	NC
209	ib_w	Track&Hold bias current	NC
210	vdd_fsb	FSB power	VDD
ib_otaq			
211	gnd_fsb0	FSB ground	GND
212	ib_sum	Preamplifier sum current bias	NC
213	EN_otaq	Enable of the multiplexed analogue output	Input
214	sum8	Sum output	NC
215	out_q	Multiplexed analogue output	Output pin test: a buffer should be added to see the waveform at scope
216	sum7	Sum output	NC
217	gnd_capa	Track &Hold ground	GND
218	sum6	Sum output	NC
219	gnd_ss	Slow shaper ground	GND
220	sum5	Sum output	NC
221	vdd_ss	Slow Shaper power	VDD
222	sum4	Sum output	NC
223	vdd_buf1	Buffer power	VDD
224	sum3	Sum output	NC

225	vdd_otaq		VDD
226	sum2	Sum output	NC
227	gnd_otaq	Multiplexed analogue output driver OTA ground	GND
228	sum1	Sum output	NC
229	vcasc_nmos	Preamplifier voltage bias	NC
230	vbi_pa	Rx to vdda and Rx to gnd if needed	Rx to vdda and Rx to gnd if needed or NC
231	gnd_nmos	Preamplifier ground	GND
232	NC		NC
233	vdd_pa	Preamplifier power	VDD
234	Ctest	input signal for internal capacitors	input signal for internal capacitors
235	vssi	Bulk inputs	GND
236	vdd_pad	Inputs Pads Protection	VDD
237	gnd_pa	Analogue (PreAmplifier) Ground	GND
238	in<0>	Analog. Input	Input
239	in<1>	Analog. Input	Input
240	in<2>	Analog. Input	Input

Table 15 – Pin type description

8.1.2 QFP 240 package layout and mechanics



SYMBOL	LEAD COUNT; FOOT PRINT			NOTE
	240; 2.6 FP			
	MIN.	NOM.	MAX.	
A	===	===	4.10	
A1	0.25	0.35	0.45	
A2	3.20	3.40	3.60	
D	34.60 BSC			
D1	32.00 BSC			
E	34.60 BSC			
E1	32.00 BSC			
L	0.45	0.60	0.75	
e	0.50 BSC			
b	0.17	===	0.27	
b1	0.17	0.20	0.23	
c	0.09	===	0.20	
c1	0.09	===	0.16	
	Tolerances of form and position			
aaa	0.20			
bbb	0.20			
ccc	0.08			
ddd	0.08			

Figure 32 - QFP 240 mechanical drawing

8.2 TF-BGA 353 package

Better description about the pins can be referred at Table 15.

8.2.1 Ballmap

	1	2	3	4	5	6	7	8	9	10	11	12
A	in<3>	in<2>	in<1>	in<0>	vbi_pa	vcasc_nmos	sum5	sum6	sum7	out_q	ib_sum	ib_otaq
B	in<5>	in<4>	N/C	ctest	sum1	sum2	sum3	sum4	N/C	sum8	EN_otaq	ib_w
C	in<7>	in<6>										
D	in<9>	in<8>										
E	in<12>	in<11>			in<10>	VDDA	VDDA	VDDA	vbo_fsb	VDDA	vddd	VH
F	in<15>	in<14>			in<13>	VDDA	VDDA	VDDA	VDDA	VDDA	vddd	vddd
G	in<18>	in<17>			in<16>	VDDA						
H	in<21>	in<20>			in<19>	VDDA		vss	vss	vss	vss	vss
J	in<24>	in<23>			in<22>	VDDA		vss	vss	vss	vss	vss
K	in<27>	in<26>			in<25>	VDDA		vss	vss	vss	vss	vss
L	in<30>	in<29>			in<28>	VDDA		vss	vss	vss	vss	vss
M	in<32>	in<31>			VDDA	VDDA		vss	vss	vss	vss	vss

Figure 33 – North-East side

N	in<35>	in<34>			in<33>	VDDA		vss	vss	vss	vss	vss
P	in<38>	in<37>			in<36>	VDDA		vss	vss	vss	vss	vss
R	in<41>	in<40>			in<39>	VDDA		vss	vss	vss	vss	vss
T	in<44>	in<43>			in<42>	VDDA		vss	vss	vss	vss	vss
U	in<47>	in<46>			in<45>	VDDA						
V	in<50>	in<49>			in<48>	VDDA	VDDA	VDDA	VDDA	VDDA	VDDA	VDDA
W	in<53>	in<52>			in<51>	VDDA	VDDA	VDDA	vcasc_pmos	VDDA	VDDA	VDDA
Y	in<55>	in<54>										
AA	in<57>	in<56>										
AB	in<59>	in<58>	N/C	D_SC	RSTn_SC	ibi_ss	ibo_ss	vref_ss	CK_R	RSTb_R	D_R	ibi_dac
AC	in<63>	in<62>	in<61>	in<60>	CK_SC	vgain_pa	ibi_buf	Qbuf_R	Hold1	Hold2	ibo_dac	iref_dac
	1	2	3	4	5	6	7	8	9	10	11	12

Figure 34 - South-East side

13	14	15	16	17	18	19	20	21	22	23	
vref_fsb	vb_otafsu	v_bg	vth0	vth1	CK_40M	CKb_40M	out<0>	out<1>	out<2>	out<3>	A
vbi_fsb	out_fs	Qbuf_SC	OR_1	OR_2	vss	vss	RSTn_ADC	N/C	out<4>	out<5>	B
									out<6>	out<7>	C
									out<8>	out<9>	D
VH	VH	VL	VL	VL	vddd	out<10>			out<11>	out<12>	E
vddd	vddd	vddd	vddd	vddd	vddd	out<13>			out<14>	out<15>	F
					vddd	out<16>			out<17>	out<18>	G
vss	vss	vss	vss		vddd	out<19>			out<20>	out<21>	H
vss	vss	vss	vss		vddd	out<22>			out<23>	out<24>	J
vss	vss	vss	vss		vddd	out<25>			out<26>	out<27>	K
vss	vss	vss	vss		vddd	out<28>			out<29>	out<30>	L
vss	vss	vss	vss		vddd	vddd			out<31>	out<32>	M

Figure 35 - North-West side

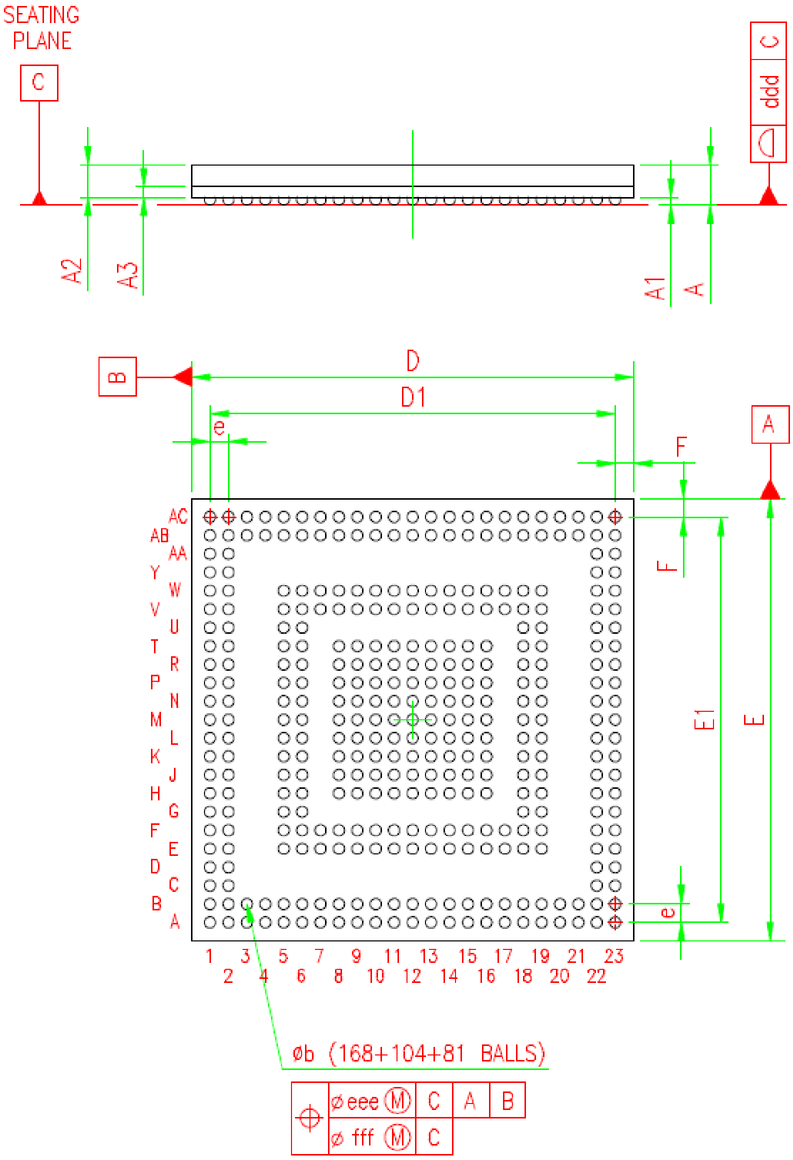
vss	vss	vss	vss		vddd	out<33>			out<34>	out<35>	N
vss	vss	vss	vss		vddd	out<36>			out<37>	out<38>	P
vss	vss	vss	vss		vddd	out<39>			out<40>	out<41>	R
vss	vss	vss	vss		vddd	out<42>			out<43>	out<44>	T
					vddd	out<45>			out<46>	out<47>	U
VDDA	VDDA	vddd	vddd	vddd	vddd	out<48>			out<49>	out<50>	V
VDDA	VDDA	vbo_discri	vddd	TransmitON	vddd	out<51>			out<52>	out<53>	W
									out<54>	out<55>	Y
									out<56>	out<57>	AA
vbi_tz	vcasc_fsu	vref_fsu	ramp	ib_integ	vbm_discri	start_ADCb	N/C	N/C	out<58>	out<59>	AB
vref_dac	G_diode	vbo_tz	vslope	vref_ramp	vbi_discri	out_ADC	out<60>	out<61>	out<62>	out<63>	AC
13	14	15	16	17	18	19	20	21	22	23	

Figure 36 - South-West side

8.2.2 Pin type description

Please refer to Table 15 for pin description.

8.2.3 TF-BGA 353 package layout and mechanics



DIMENSIONS

SYMBOL	MILLIMETER		
	MIN.	NOM.	MAX.
A			1.20
A1	0.15		
A2		0.88	
A3		0.28	
b	0.25	0.30	0.35
D	11.85	12.00	12.15
D1		11.00	
e		0.50	
E	11.85	12.00	12.15
E1		11.00	
F		0.50	
ddd			0.08
eee			0.15
fff			0.05

Figure 37 – TF-BGA 353 mechanical drawing

9 Bug list & hotfix log

- Maroc3A update :
  - Slow Control register output (pin 199 or B15) presented at clock falling edge
  - Wilkinson ADC slope modifications (Hotfix for MAROC3 is done directly on evaluation board – 180k Ohm between Pin 95 and VDD)

10 Document version

Version	Date	Pages	Changelog
1.0	20/06/2017	29	Initial release
1.1	28/08/2017	45	Updated info