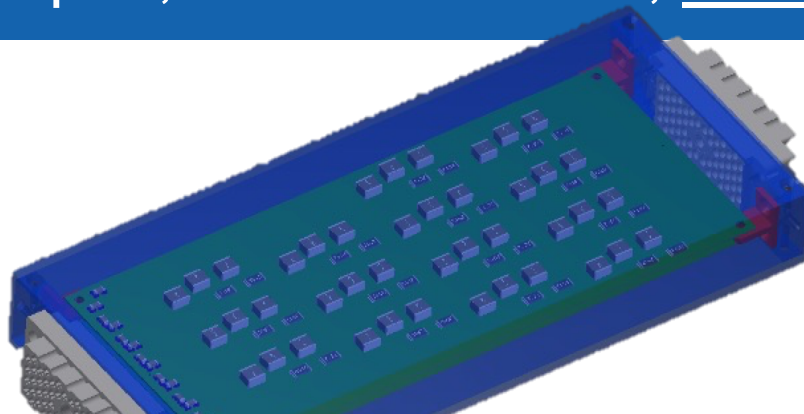


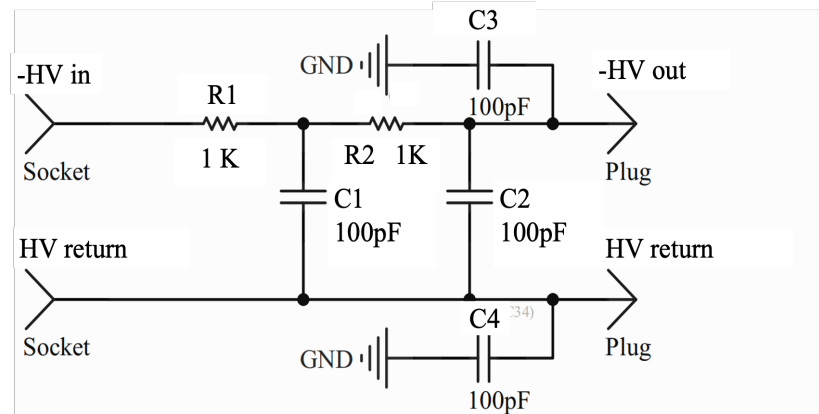
HGTD HV Patch Panels Status

Luis Lopes, Orlando Cunha, Ricardo Gonalo



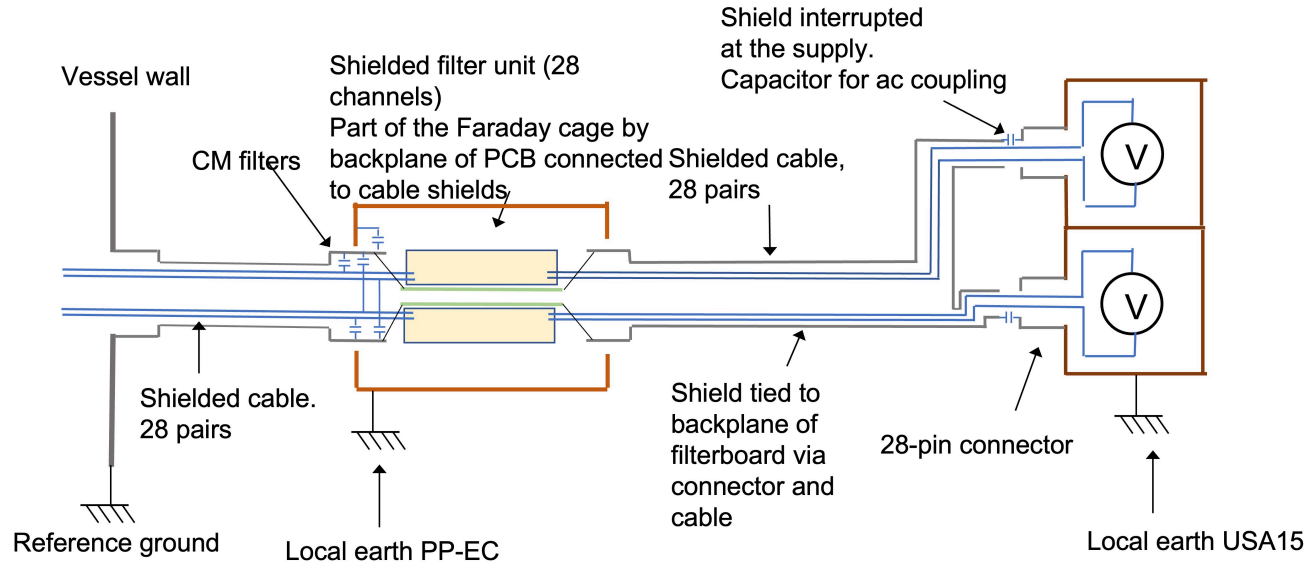
Patch Panel Filter Design For PDR

- HV routing through fixed wire connections between input long cables from USA15 and short cables to detector modules
- 2nd order RC-RC low-pass filter to suppress AC noise
 - Up to -900 V with, no significant leakage, supply currents up to 3 mA per channel
- Decoupling capacitors to suppress common-mode noise (C3, C4)



Patch Panel Filter Design For PDR

- Differential HV channels, insulated from the patch panel unit
 - Module aluminium boxes act as Faraday cage, electrically connected to the Tilecal surface
 - HGTD earth extends through cable sleeve to filter board backplanes
 - HGTD/Filter earth insulated from module earth (=Tilecal earth) to avoid ground loops

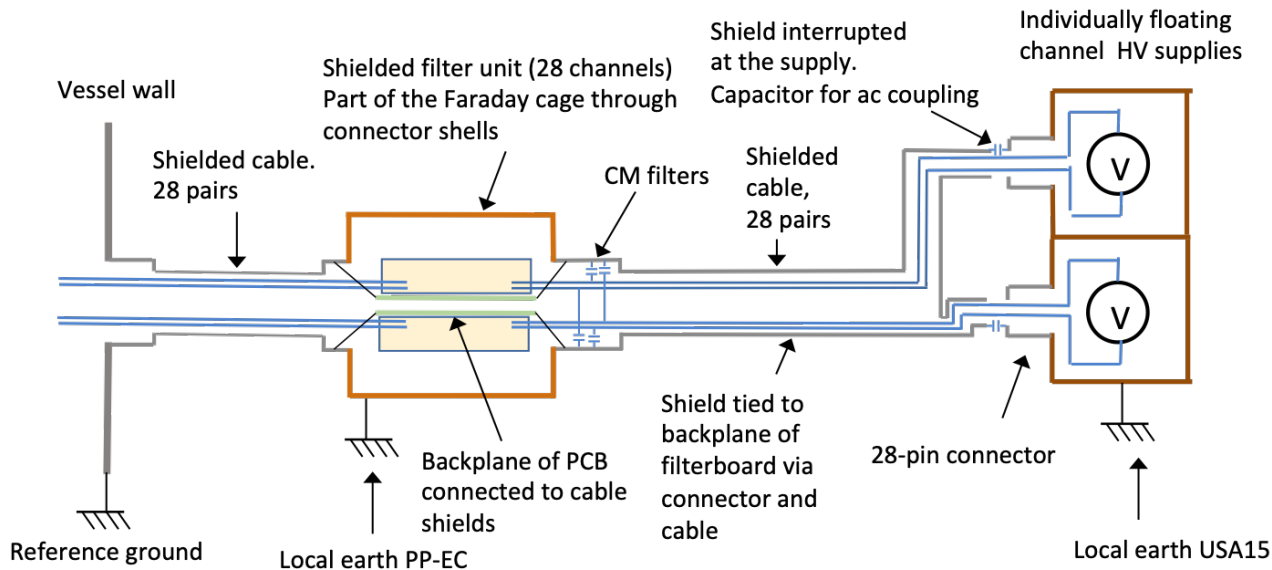


PDR Discussion and Updates

- HV PDR meeting on 29 August: <https://indico.cern.ch/event/1190013/>
- Questions raised by Vincent Bobillier on grounding scheme and best way to suppress noise
 - Suggested a discussion with Georges Blanchot, electronics engineer at CERN
- Proposal for changed design in next page

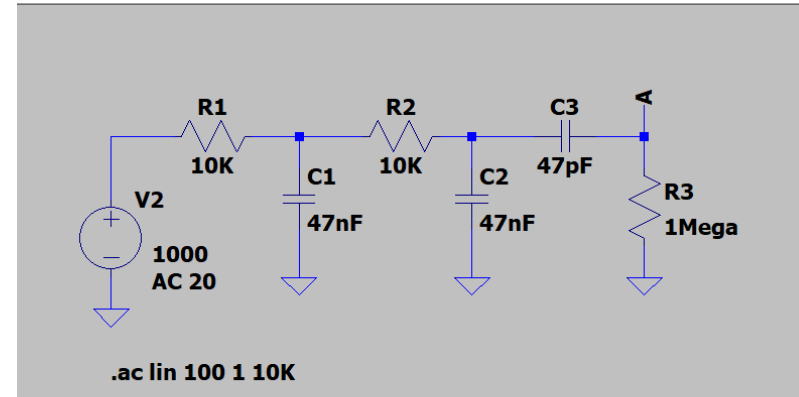
Proposed Changes

- Use filter module boxes as continuation of vessel Faraday cage
 - Also DC connection of filter boards backplane to cage
- DC connection of Faraday cage to local TileCal earth
 - DC current not as bad as HF AC noise
- Move common-mode filter capacitors to filter input instead of output
 - Filter common mode current at input



Prototype tests and quality control

- Planned tests:
 - Connectivity of components and filter performance tested by measuring the filter response as function of frequency and load
 - Leakage current
 - Insulation between internal and external ground.
 - Cross talk between channels
 - Temperature under load
 - Long term reliability including enhanced aging by temperature cycling in a climate chamber
 - Radiation and magnetic field tolerances
- For production:
 - Based on prototype results will establish set of quality control benchmarks to be done in production and upon delivery

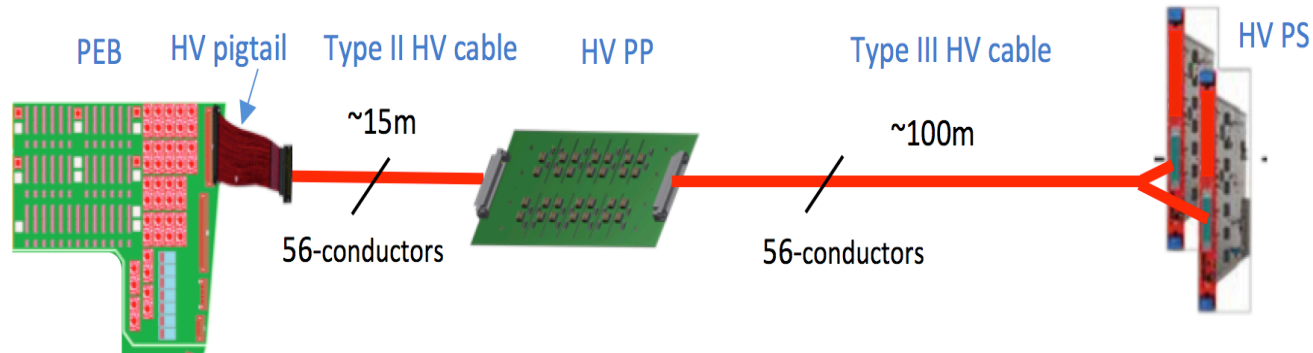


Thanks!



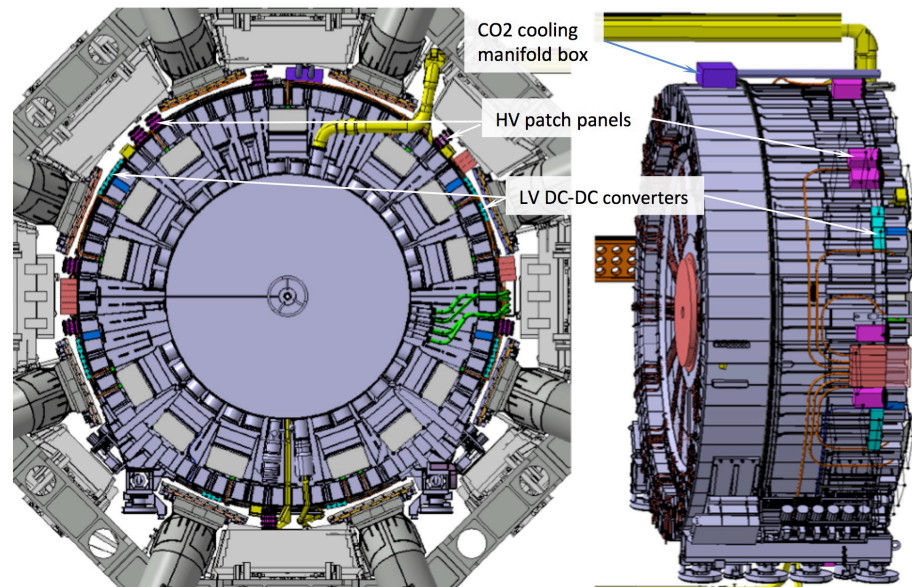
HGTD HV Patch Panels

- Each of the 8032 HGTD modules will need a bias voltage between -300 V and -900 V, adjusted individually
- Electronic noise induced in the DC bias voltage at the power supply or in the cables between USA15 and the detector must be filtered out.
- Filter modules (EC-PP) will be installed on the end-cap calorimeter surfaces – filter noise and allow HV channel routing



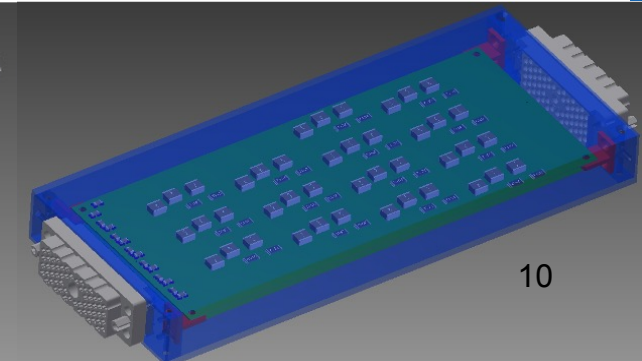
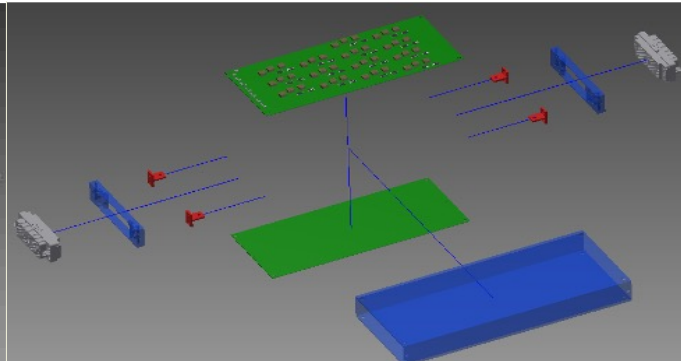
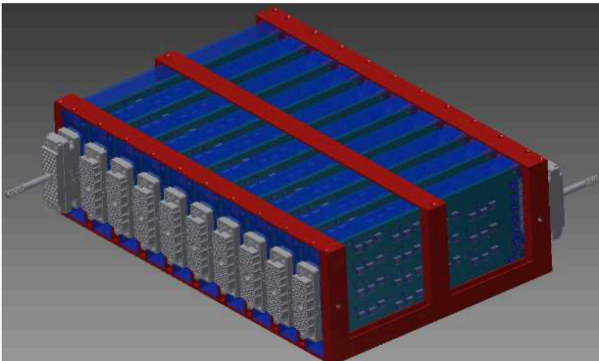
Patch Panel design parameters

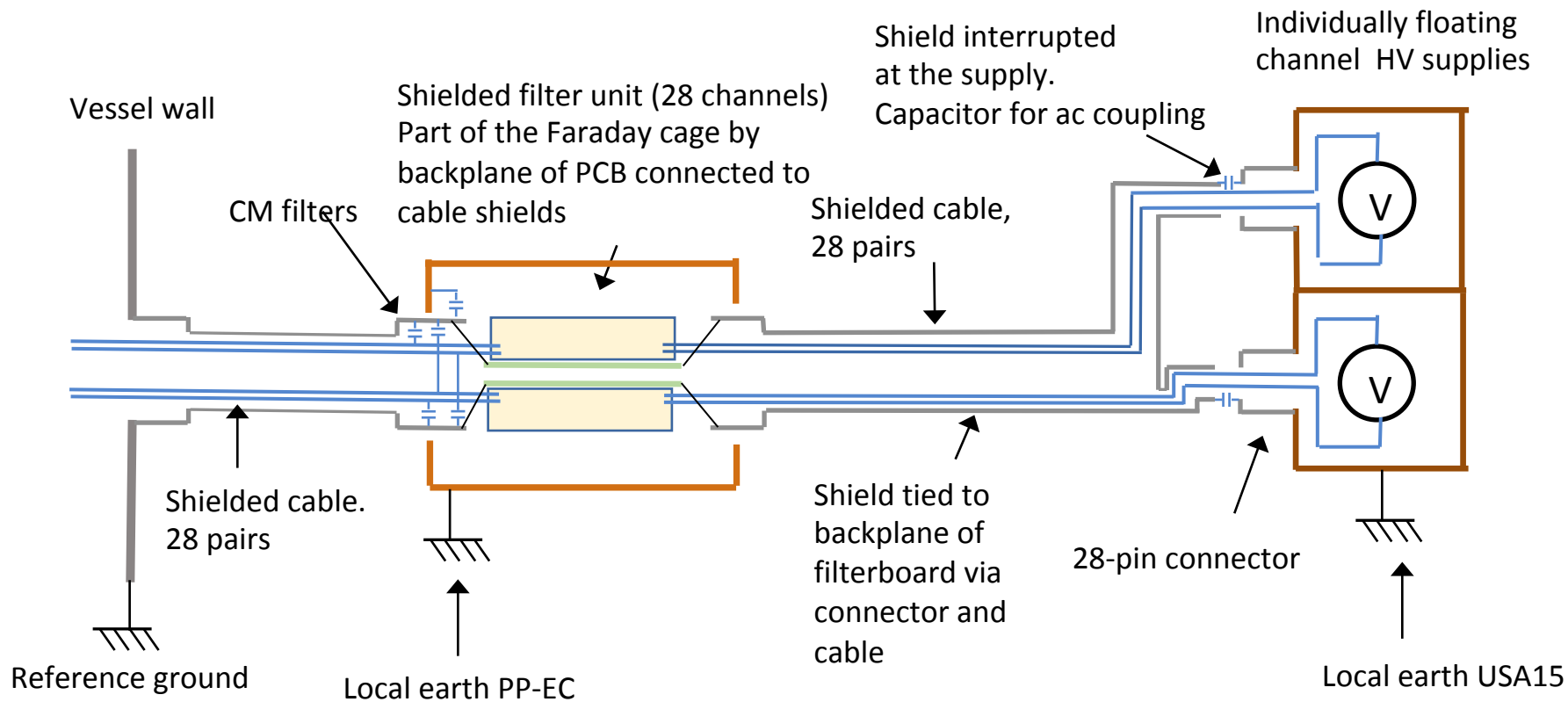
- Materials to withstand radiation and magnetic field:
 - TID 15.0 Gy and 1 MeV neq fluence $1.0 \times 10^{12} \text{ cm}^{-2}$
 - Magnetic field up to 0.5 Tesla
 - Avoid easily activated and magnetic materials
 - Avoid extensive use of dielectrics
- Mechanical stability and ease of access during shutdowns
 - Robust connectors
 - Fixation to Tilecal and cable strain relief staves – to be studied together with Technical Coordination
- Space constraints
 - Around 20cm free in radial direction
- Number of wires should present good match to cables from HV supplies

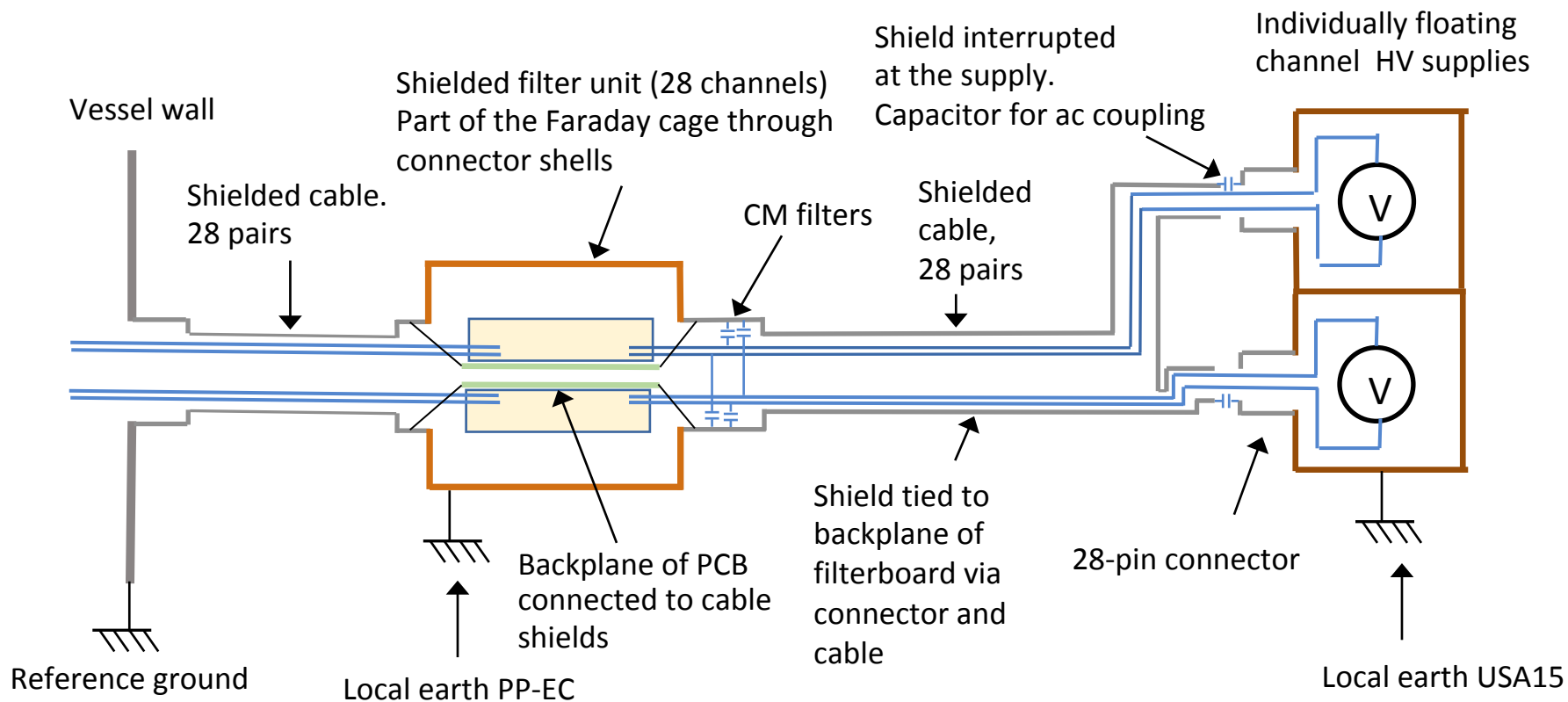


Patch Panel Units Design

- A modular design is proposed for the patch panels
- Individual modules are aluminium boxes containing two filter boards and connectors
 - Provide mechanical support and insulate each pair of boards within separate Faraday cage
 - Easy to construct, handle and access for maintenance
 - 14 RC-RC low-pass filters in each filter board
 - Means one 56-wire cable connected to each module: = 28 HV channels = 14 channels x 2 boards
 - Routing of individual HV channels through wires connecting cables to each filter board







Initial (pre-)prototype tests

RC–RC filter: 10 k Ω x 33 nF or 47 nF

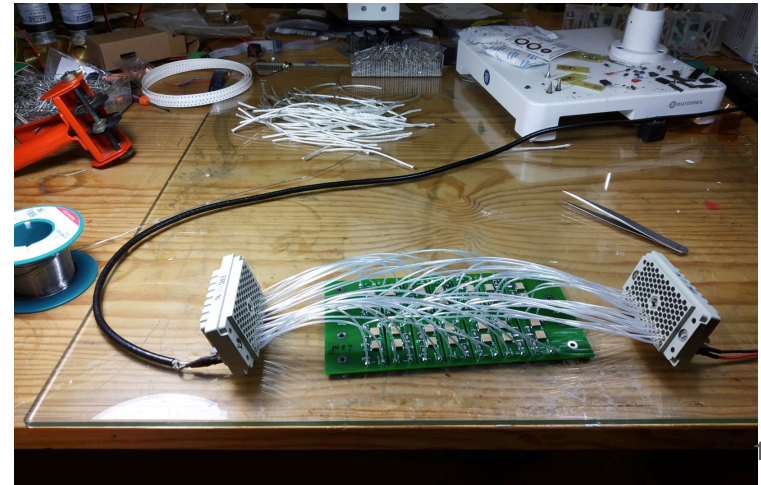
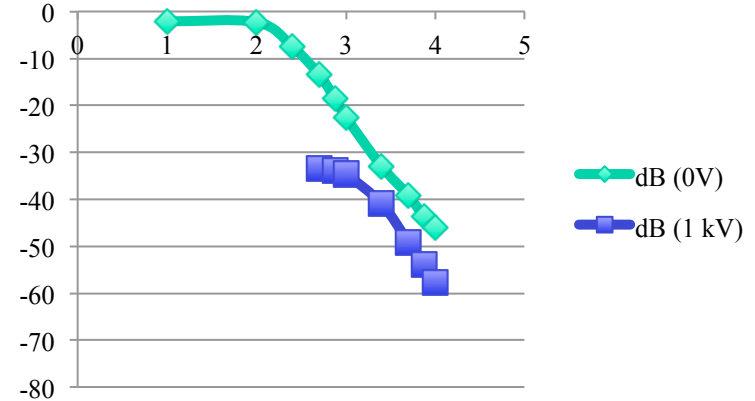
- Note R and C not final – must be defined together with sensors and tested together

Assuming 3 mA maximum current means:

- 60 V voltage drop
- 180 mW max. dissipation per channel
- I.e. 5 W / 24-channel box

Ideal response:

- $f_c = 338$ Hz (33 nF) or 482 Hz (47 nF)
- -40 dB / decade
- Achieved this when tested inside shielding box



Prototype tests

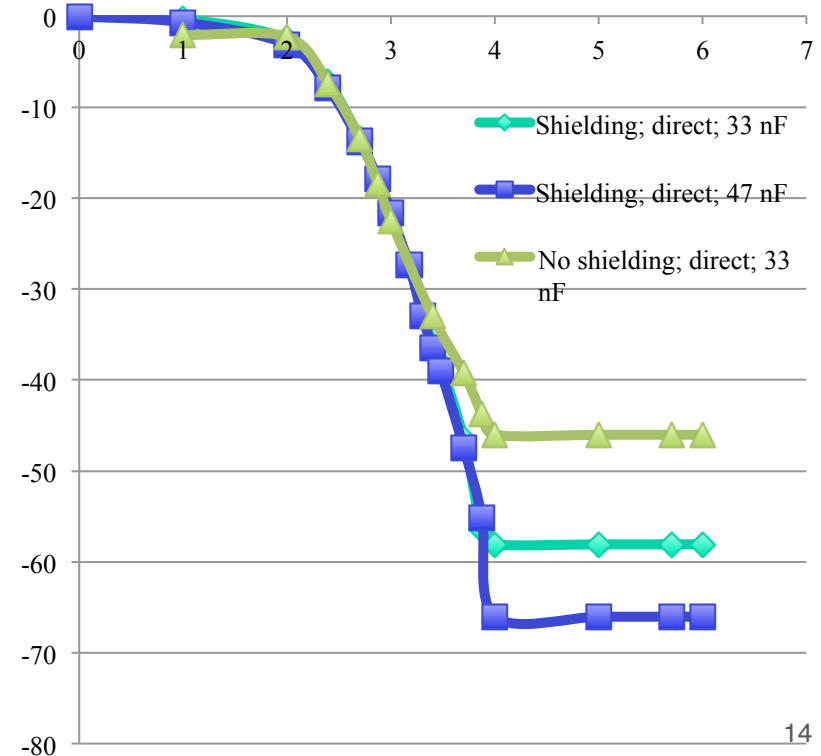
Response improves with shielding (Faraday cage)

- Closer to -40 dB / decade

Response flat above 10 kHz

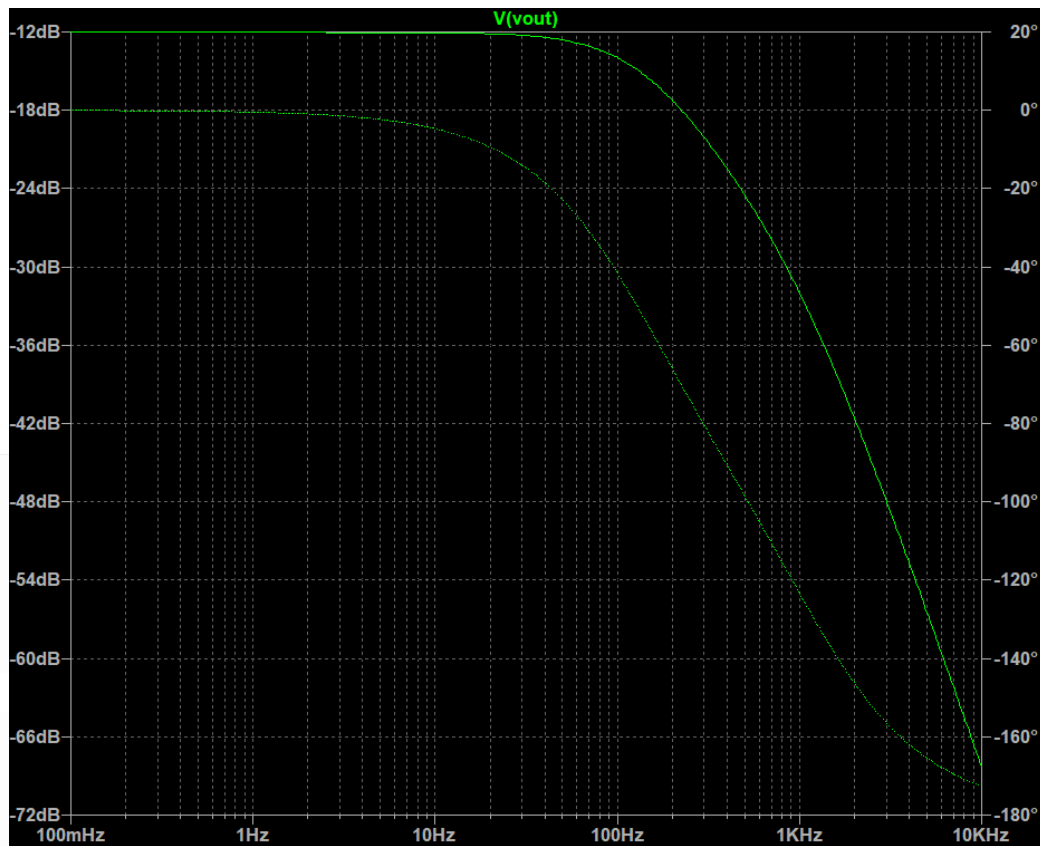
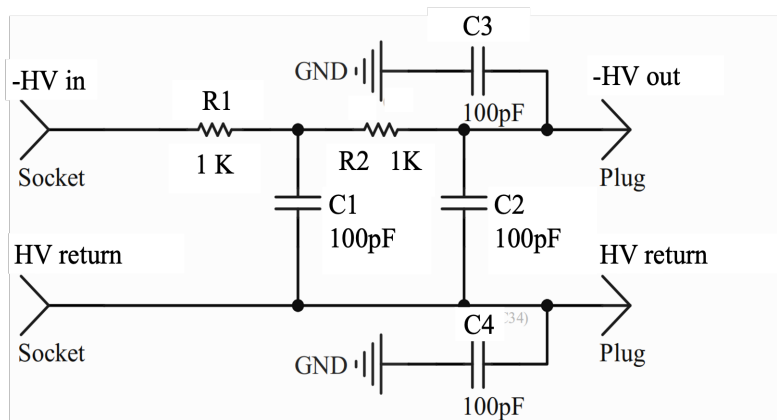
Other tests foreseen:

- Leak current under HV bias – waiting for precision HV module to be free, to ease measurement
- Final tests must be done with HGTD HV source prototype



Response curve

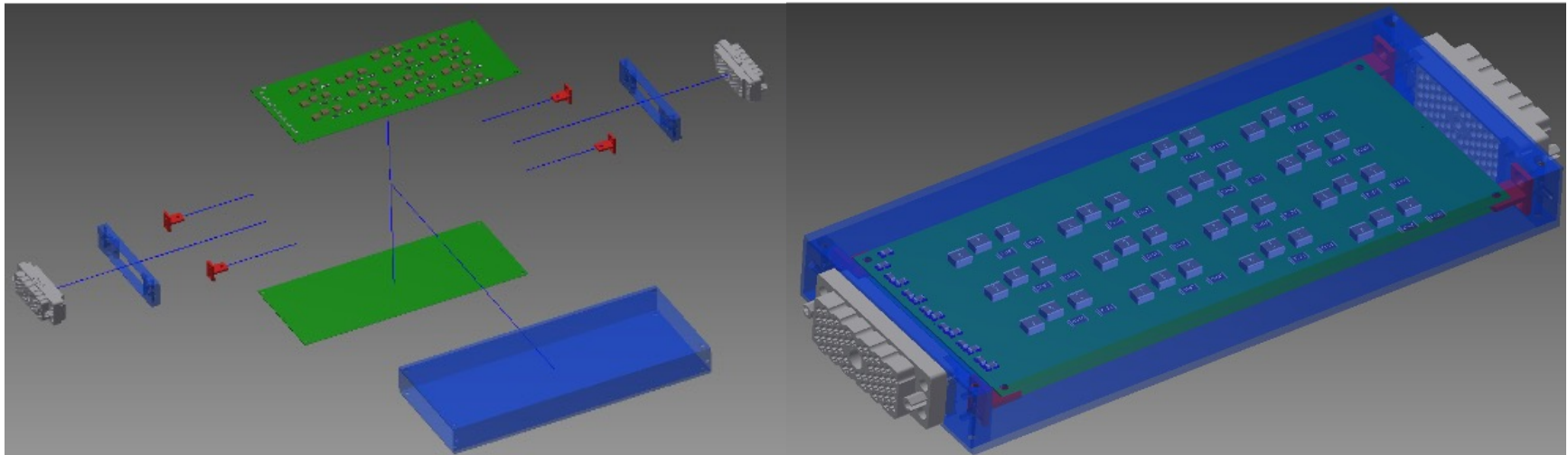
Response after adding common-mode decoupling capacitors



Optimising design

Also tried an alternative design to:

- Ease assembly: reduces production time and manufacture errors
- Improve robustness: assess robustness of routing cables / soldering
- Add decoupling capacitors against common-mode noise in each channel
- Lower cost:
 - Especially by reducing length of cable for HV routing
 - Trying routing in 4-layer PCB



Connectors

Found potentially interesting connectors from Farnell:

<http://www.farnell.com/datasheets/2916873.pdf>

Unit price (120 pins, small quant.): 53 € plug; 45 € pins; 26 € connector

To be used for this prototype and replaced later



516 SERIES

RACK AND PANEL CONNECTOR (PLUG AND RECEPTACLE)

Specifications:

Insulator Material	Diallyl Phthalate, Thermoplastic Polyester or Polycarbonate UL 94V- 0
Color	Green or Grey
Contact Material	Copper Alloy
Contact Plating	Gold Plating over Nickel over entire contact
Current Rating	8.5 Amperes
Contact Resistance	10 milliohms maximum
Withstanding Voltage	2000 VAC rms at sea level
Insulation Resistance	5000 Megaohms minimum
Operating Temp	-40°C to +125°C (Diallyl Phthalate Only)
Operating Temp	-40°C to +105°C
Insertion & Withdrawal Force	2 to 16 Oz (0.56 to 4.45N) per contact position ¹⁷

Measurements

Difficult to measure
low-frequency
behaviour with our
current setup due to
output capacitor in
waveform generator

