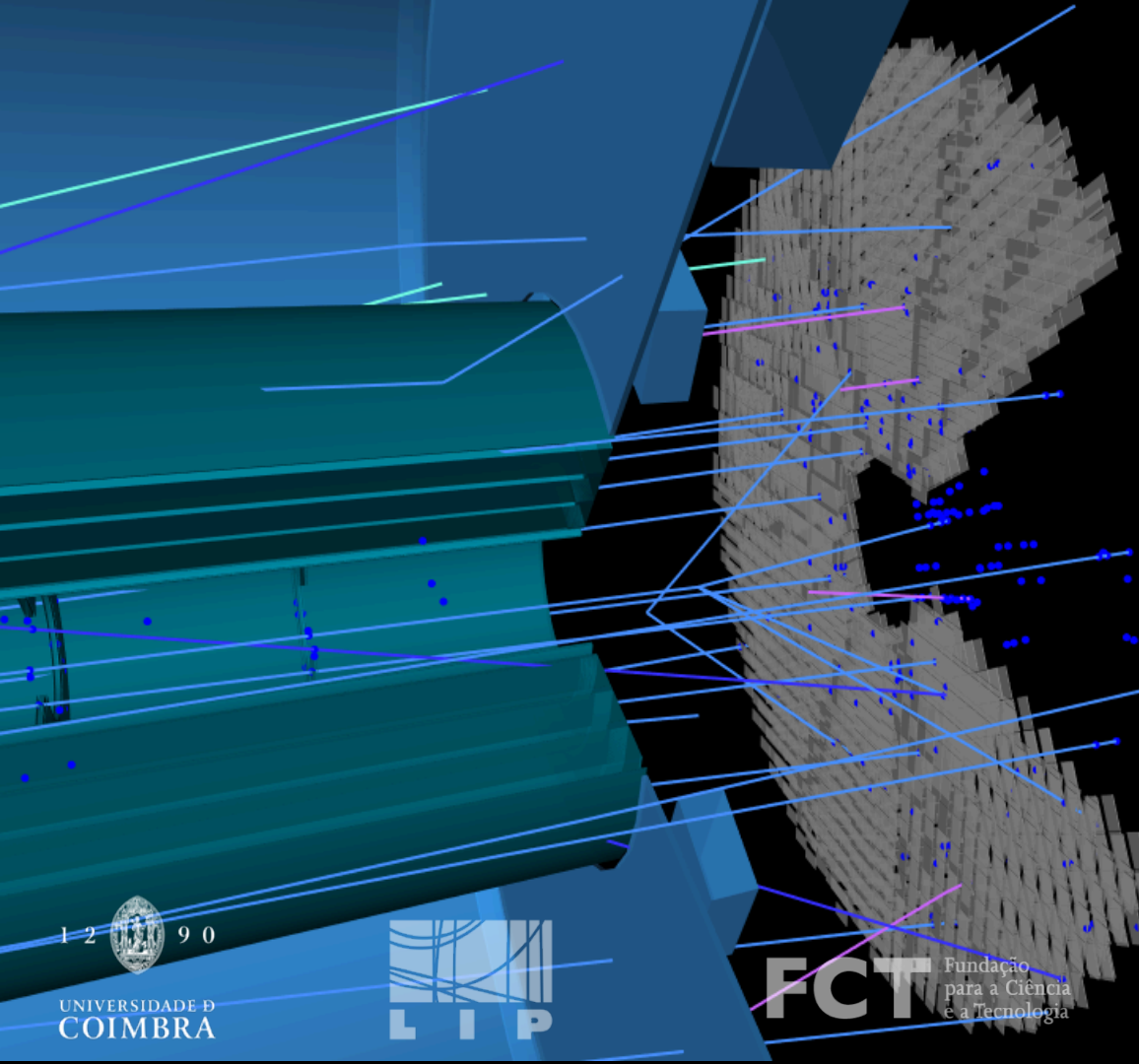


High Granularity Timing Detector

Ricardo Gonçalo (U. Coimbra, LIP)
on behalf of the HGTD Group

ATLAS Week, Lisbon, October 2022

UNIVERSIDADE D COIMBRA

LIP

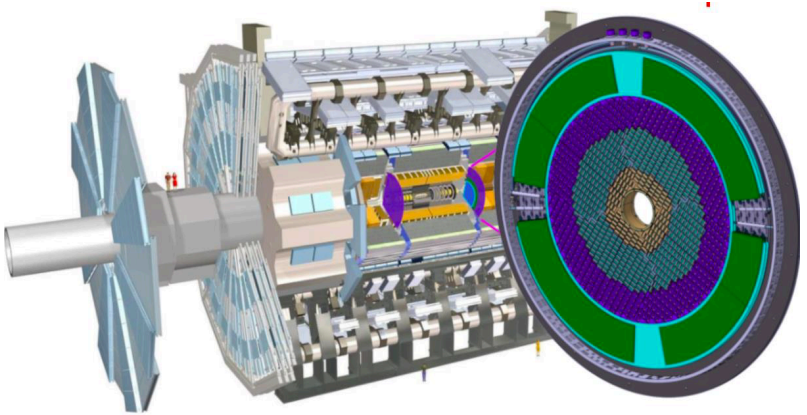
FCT Fundação para a Ciência e a Tecnologia

ATLAS EXPERIMENT

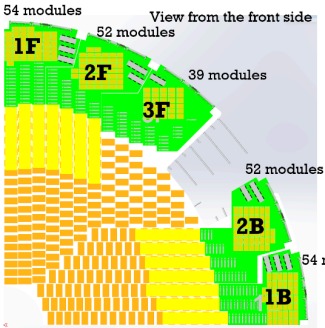
CERN

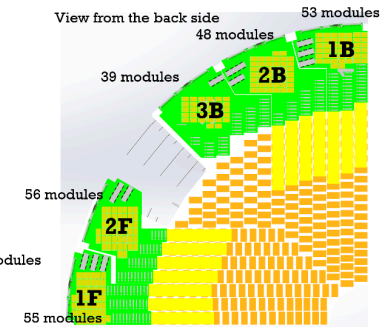
The High Granularity Timing Detector

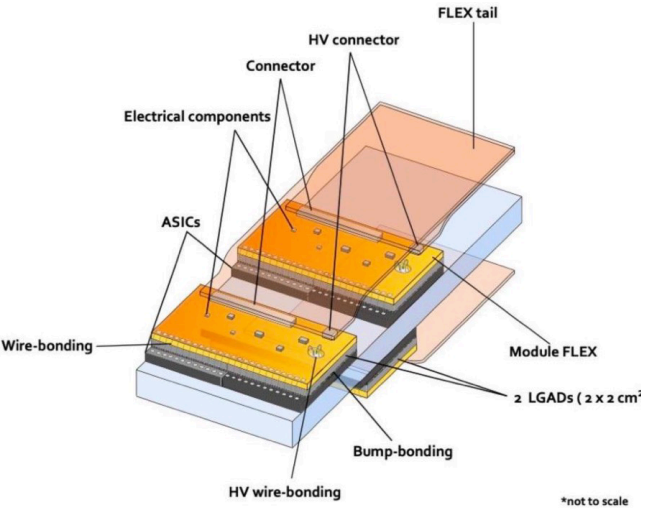
- Two detector wheels between ITk and endcap:
  - **z = ±3.5 m**; 7.5 cm thick (+5 cm neutron moderator)
  - Active detector region: **2.4 < |η| < 4.0**
  - 8032 **modules** with 2 **hybrids** each (sensor + readout ASIC)
  - 3.6 M channels; 1.3×1.3 mm^2 pixels; 6.4 m^2 active area
  - Radiation hardness: **up to 2.5x10^{15} Neq /cm^2**, **2 MGy**

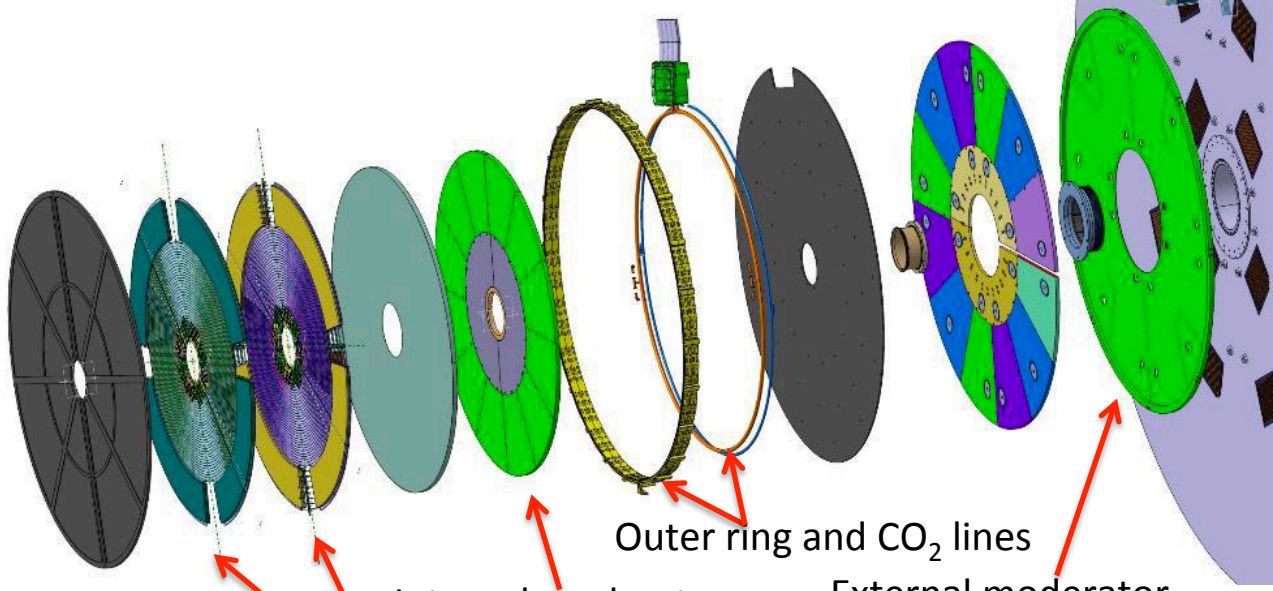


- **Pileup** rejection:
  - Identify track vertex in forward region (poor ITk z_{VTX} resolution)
  - **30-50 ps/track**, 35-70 ps/hit resolution
- **Luminosity** measurement:
  - Count number of hits at 40 MHz to get bunch-by-bunch luminosity
  - Goal is **1% luminosity uncertainty**



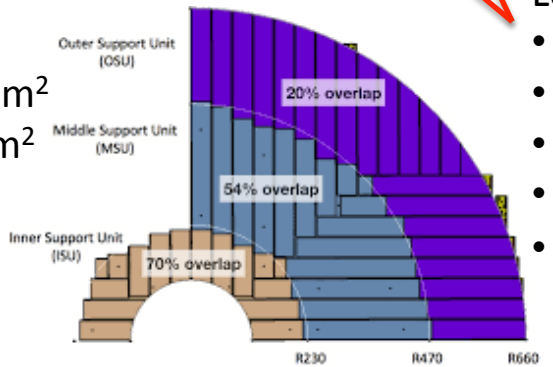






HGTD **Modules**:

- LGADs **bump-bonded** to two ALTIROC ASICs: 2×2 cm^2
- 15×15 pads of 1.3×1.3 mm^2
- Operated at **-30 °C** (CO_2 cooling) to cope with radiation damage

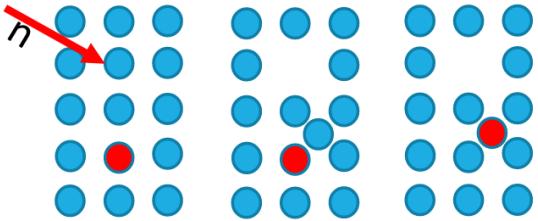


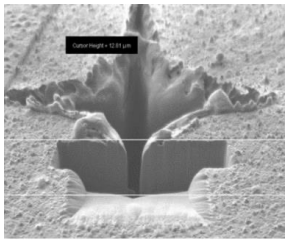
Low Gain Avalanche Detector (**LGAD**) sensors:

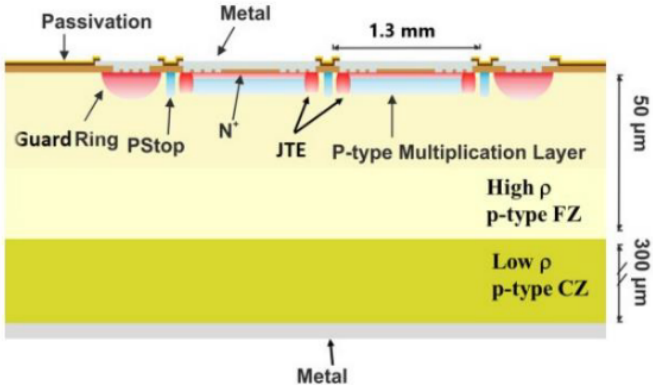
- Mounted on **both sides** of cooling disks
- **Active** region: 12 cm < r < 64 cm
- **Peripheral electronics**: 64 cm < r < 100 cm
- Three regions with different **sensor overlap**
- **Neutron moderator** (5cm) to shield detector from backscattered neutrons

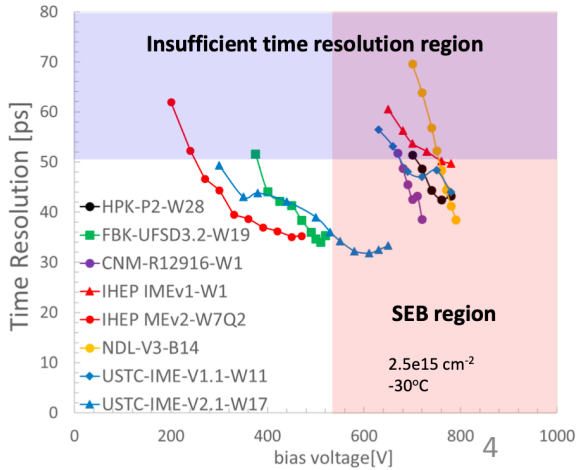
Low Gain Avalanche Detector Sensors

- Aim for 70 ps/hit timing resolution **after full irradiation**
- Thin ≈50 µm active layer on thick ≈300 µm substrate
- **Multiplication layer**
  - Affected by irradiation originated defects (acceptor removal)
  - Compensated by higher bias voltage up to a point
- **Single Event Burnout** (**SEB**) in irradiated sensors at high HV
  - Above 12 V/µm or ≈600 V/50 µm wafers
- Robustness improved by **carbon-enriched gain layer**
  - Only carbon-enriched gain layer modules viable for operation

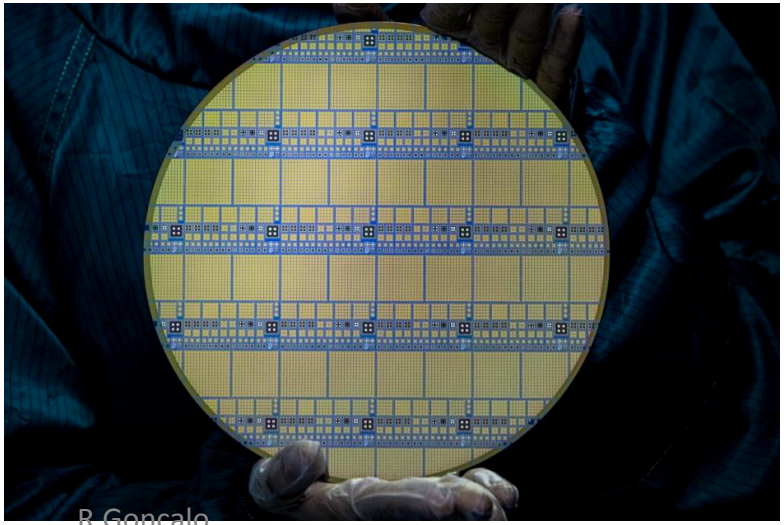


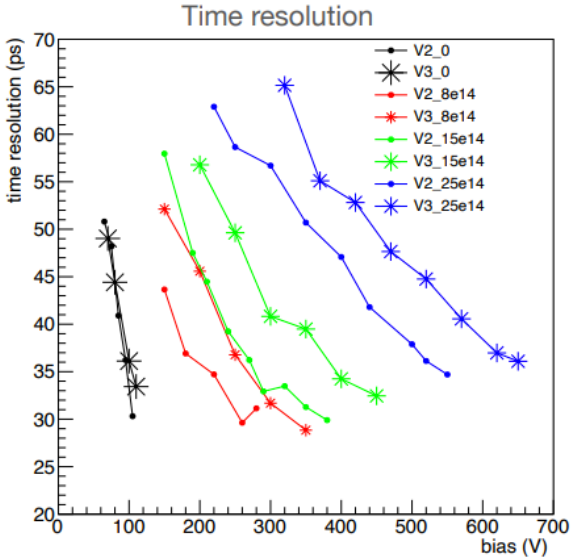


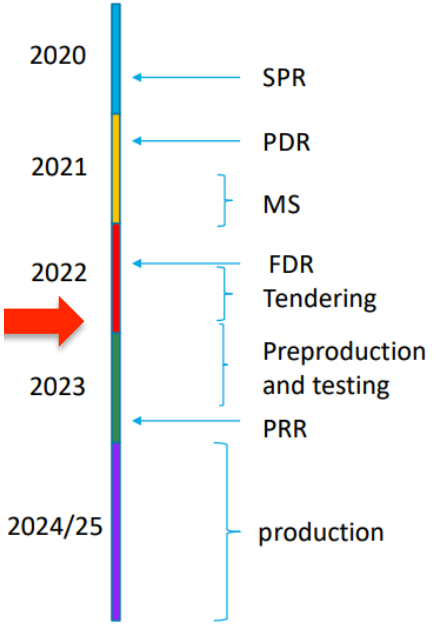




- Testing sensors from 4 different vendors − with carbon-enriched gain layer
- Test program for sensors and sensor+ALTIROC assemblies
- Sensors from at least 3 vendors satisfy the requirements to be used in HGTD
- Tendering process in preparation
  - Expect contracts awarded in December − 1.5 month delay
  - Will accelerate procedure and stagger production to avoid delays

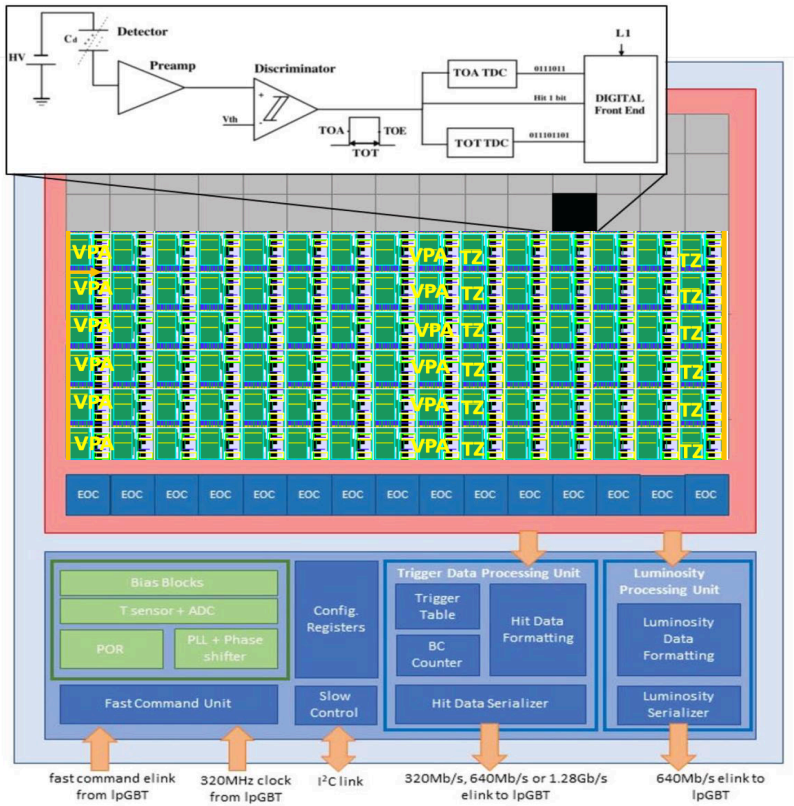




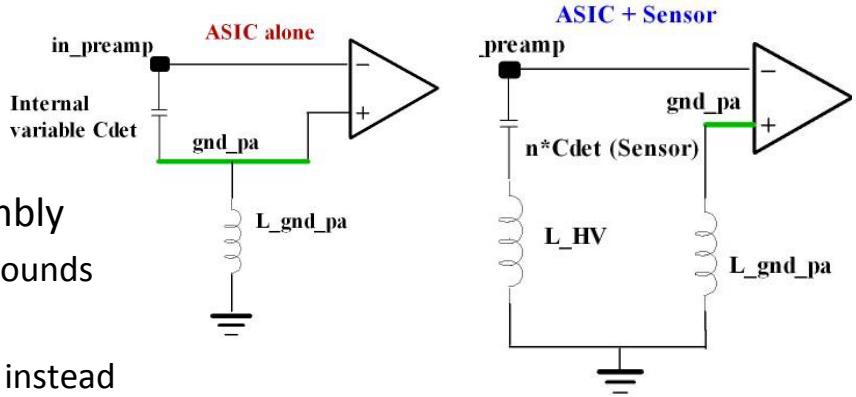


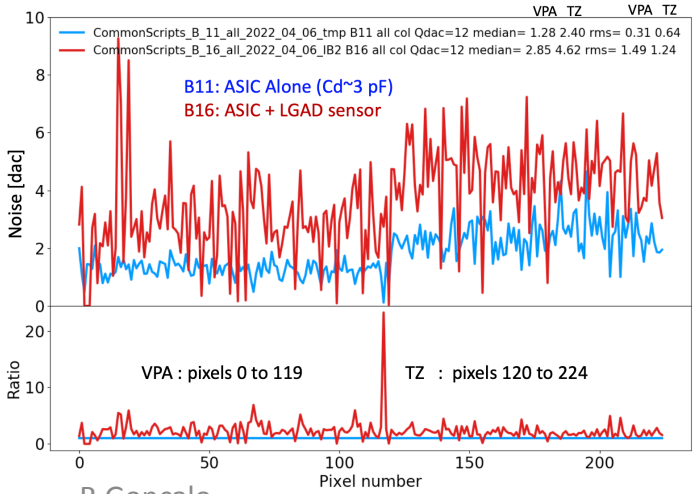
ALTIROC frontend ASIC

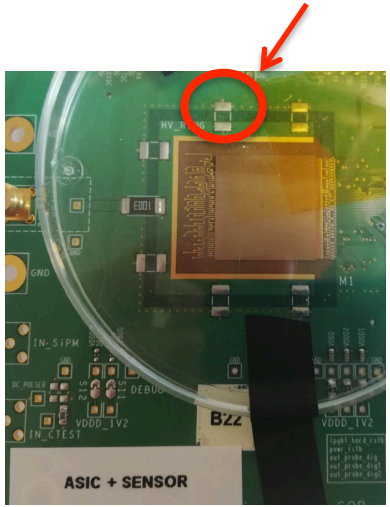
- Readout of **15×15 LGAD pixels**
- 2×2 cm^2 **bump-bonded** to sensors
- Specifications:
  - Jitter < 25ps @ 10 fC; <65ps @ 4 fC
  - Minimum threshold: 2 fC
- Outputs:
  - **Time Of Arrival** (TOA)
  - **Time Over Threshold** (TOT)
  - **Luminosity** (No. of pixels hit)
- ALTIROC 2: **first full size** prototype; tests being finalized at several institutes
- ALTIROC 3: **to be submitted** in November

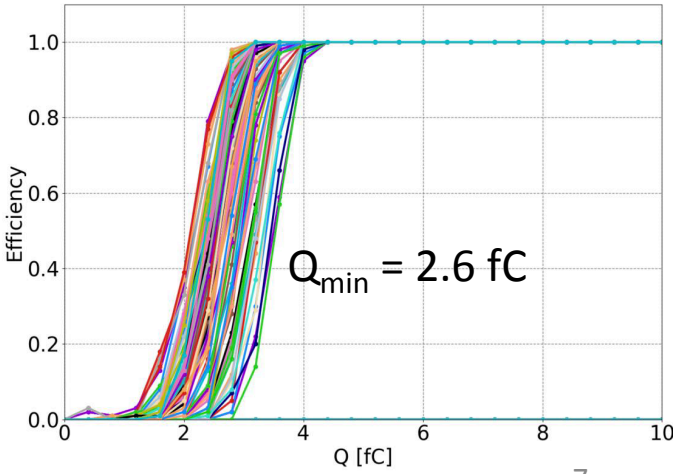


- Intensive **ALTIROC 2** testing program:
- **ASIC alone** found to be close to specifications
- But **additional noise** found in ASIC + LGAD sensor assembly
  - Due to parasitic inductances separating sensor/preamp grounds
  - Effect amplified due to 10 nF HV decoupling capacitor
  - Removing capacitor gave **lower noise** and so Q_{min} **= 2.6 fC** instead of **4 fC** with capacitor



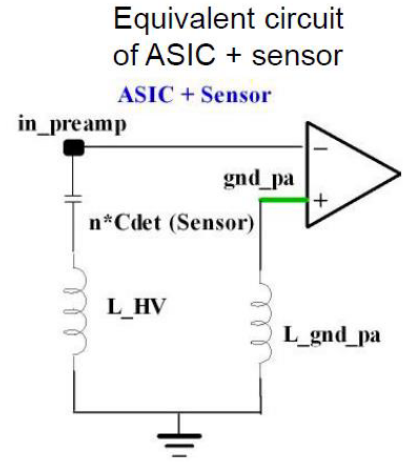


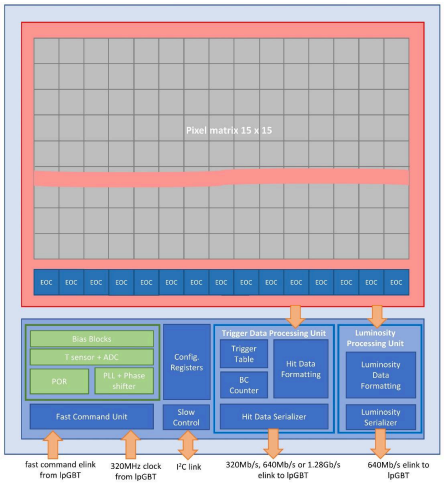




ALTIROC 3

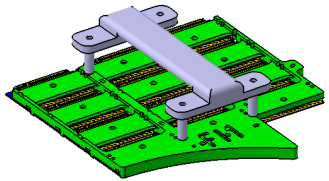
- **Improvements** with respect to ALTIROC 2:
  - Identified bottleneck for trigger rates > 1 MHz giving **high FIFO occupancy**
  - Modifications for **smaller Q_{min} and jitter** to address:
  - Voltage drops between grounds solved in ALTIROC 3
  - Digital noise injected through preamplifier ground
  - Higher redundancy to improve robustness against Single Event Effects
  - 40 MHz clocks in ALTIROC 3 matrix de-skewed along the columns and between columns to avoid high digital current spikes
- Power consumption slightly higher : 1.4 mW/ch vs 1.2 mW/ch
- ALTIROC **plans**: PDR set to October 18
  - Design of ALTIROC 3 version is now ready − verifications in coming month
  - **Submit to foundry in early November** − to arrive at CERN early Feb. 2023
- HGTD-ALTIROC-A − **pre-production** ASIC
  - Design to start in April 2023 and FDR in October 2023

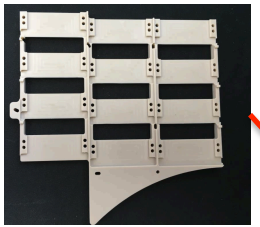


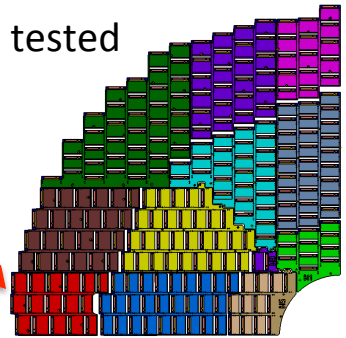


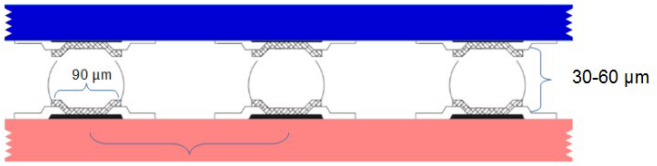
HGTD Modules

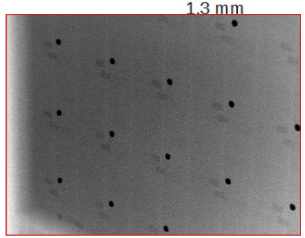
- Hybridization: Sensor bump-bonded to ASIC
  - Technique established at several sites
  - Detailed tests (shear test, X-ray examination) have shown good bonding results achieved
  - Beam tests at CERN in July and September; next one in 19/10 – 02/11
- Five full modules produced and more without sensor
  - Load to be spread between several institutes
- Dedicated tools developed:
  - Bending the flex, aligning and placing the bare module on the flex, and glueing the assembly
- Support units developed and prototypes tested

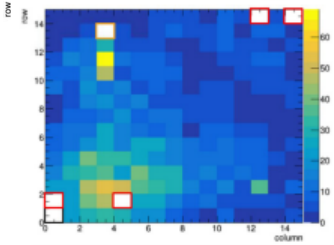


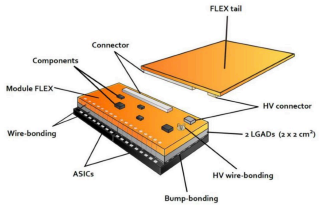


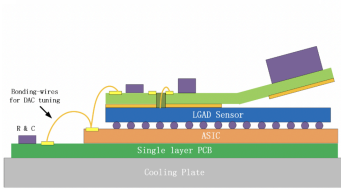


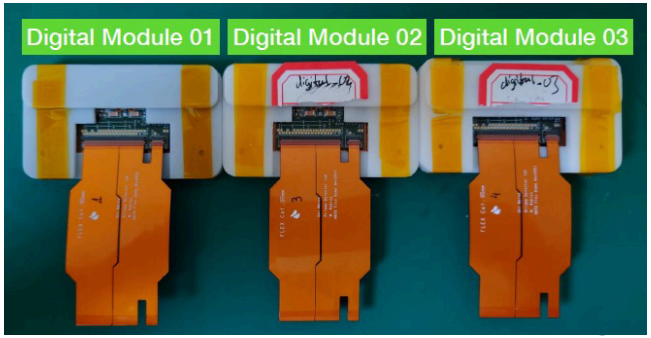






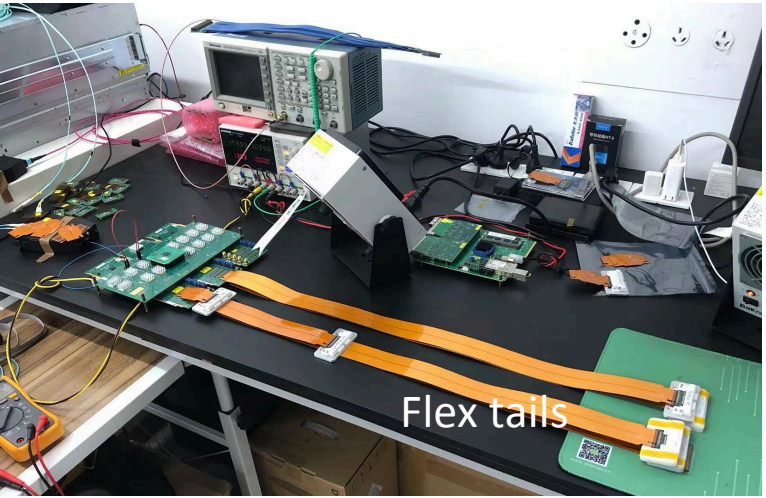


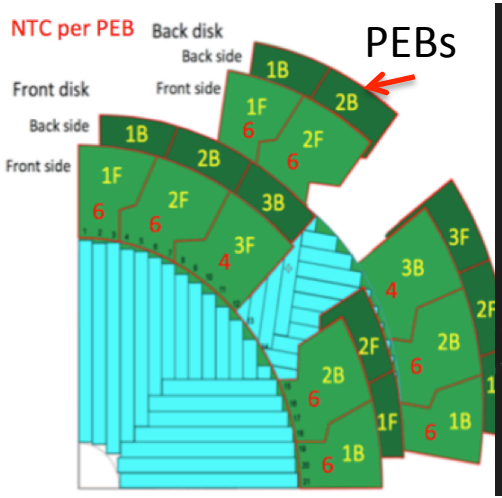


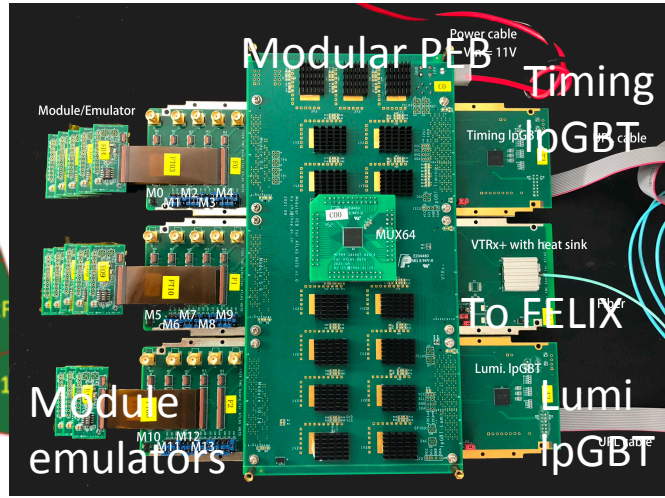


Peripheral Electronics Boards

- Prototype (PEB 1F) design to finish soon – some delays to understand communication with FELIX and to simplify PEB design, to save time/complexity later on:
  - Space limitations on rigid PCB for connectors and components required flex tails integrated into rigid PCB
  - A lot of individual testing of components (lpGBT, VTRX+) already done
- PDR in Nov 2022; PEB 1F Production: Dec 2022-Jan 2023

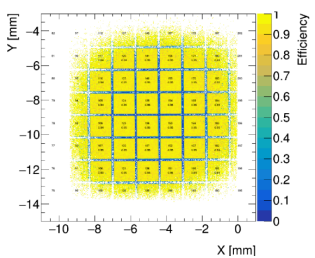


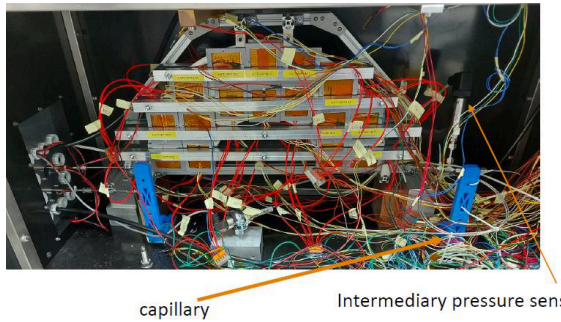


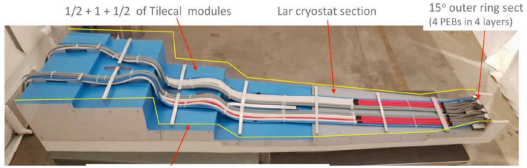


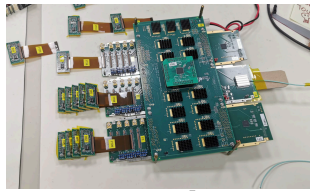
And Much Much More!...

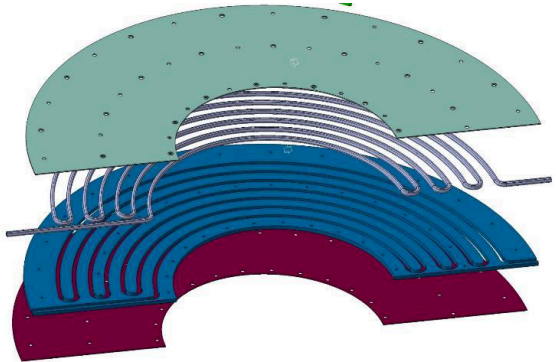
- Heater and DAQ demonstrators
- And a mockup for cable routing
- Test beams and sensor irradiation
- Full update of mechanics vessel design, ready for PDR
- DCS and Interlocks development
- Grounding and shielding
- Beamtest paper accepted: link
- Etc, etc...

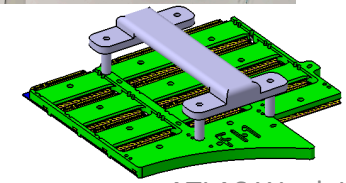


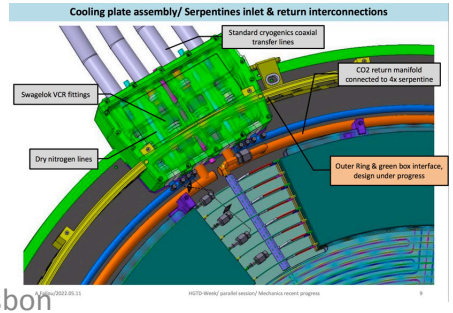


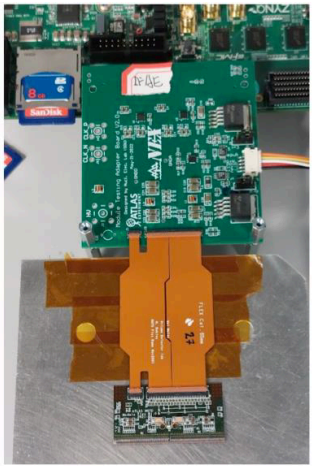












Project Overview

LGAD Sensor production: **Tendering ongoing**

- Pre-production to start in December, followed by tests

ALTIROC ASIC: **Critical, FDR October 2023**

- ALTIROC3 to be submitted early November
- Pre-production (ALTIROC A) design starts April 2023

Peripheral electronics boards: **PDR (PEB 1F) November 2022**

- Complex large boards with 6 versions – design slightly behind
- Design of other versions to start in January 2023

HV Power Supplies: **PDR passed in September 2022**

- Ordering full-size prototypes for evaluation
- PDR raised questions on gounding scheme (single-point vs mesh)

LV Power Supplies: **FDR planned for December 2022**

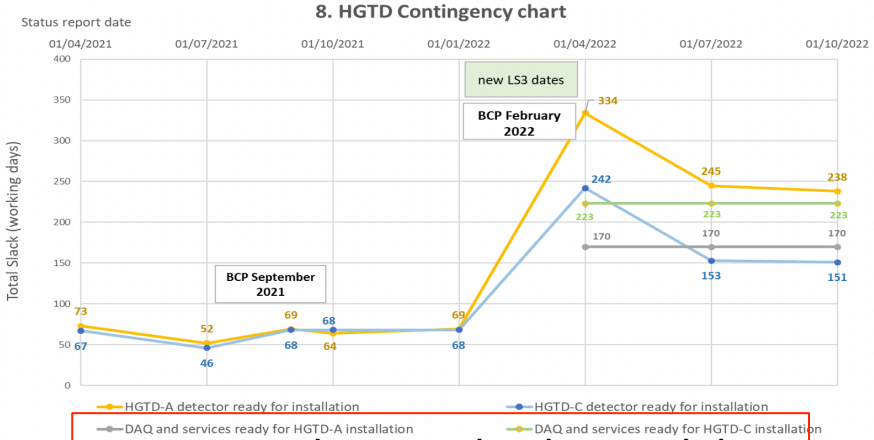
- Pre-production expected in March 2023

Modules, Flex cables, Detector units: **PDR planned for Dec 2022**

- Production of 50 modules for full demonstrator by February 2023

Mechanics and on-detector cooling: **PDR in November 2022**

Services, CO2 cooling, N2, Cables, Fibres: **PDR in November 2022**



Lost around 2 months due to delay in ASIC submission

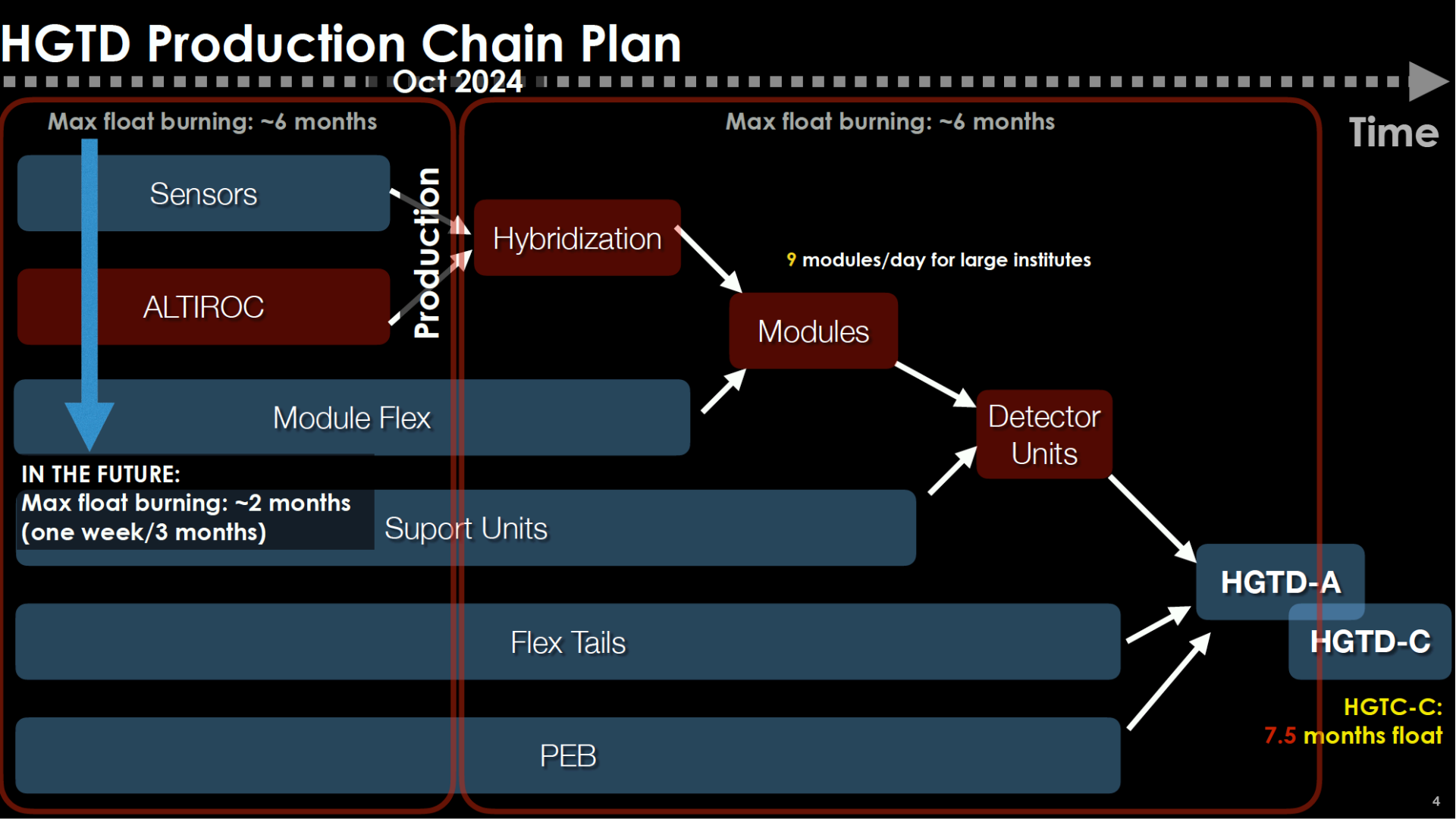
- But **delays now stabilized** – only 1 week lost in last quarter

Project **contingency**:

- HGTD-A: 238 working days
- HGTD-C: 151 working days

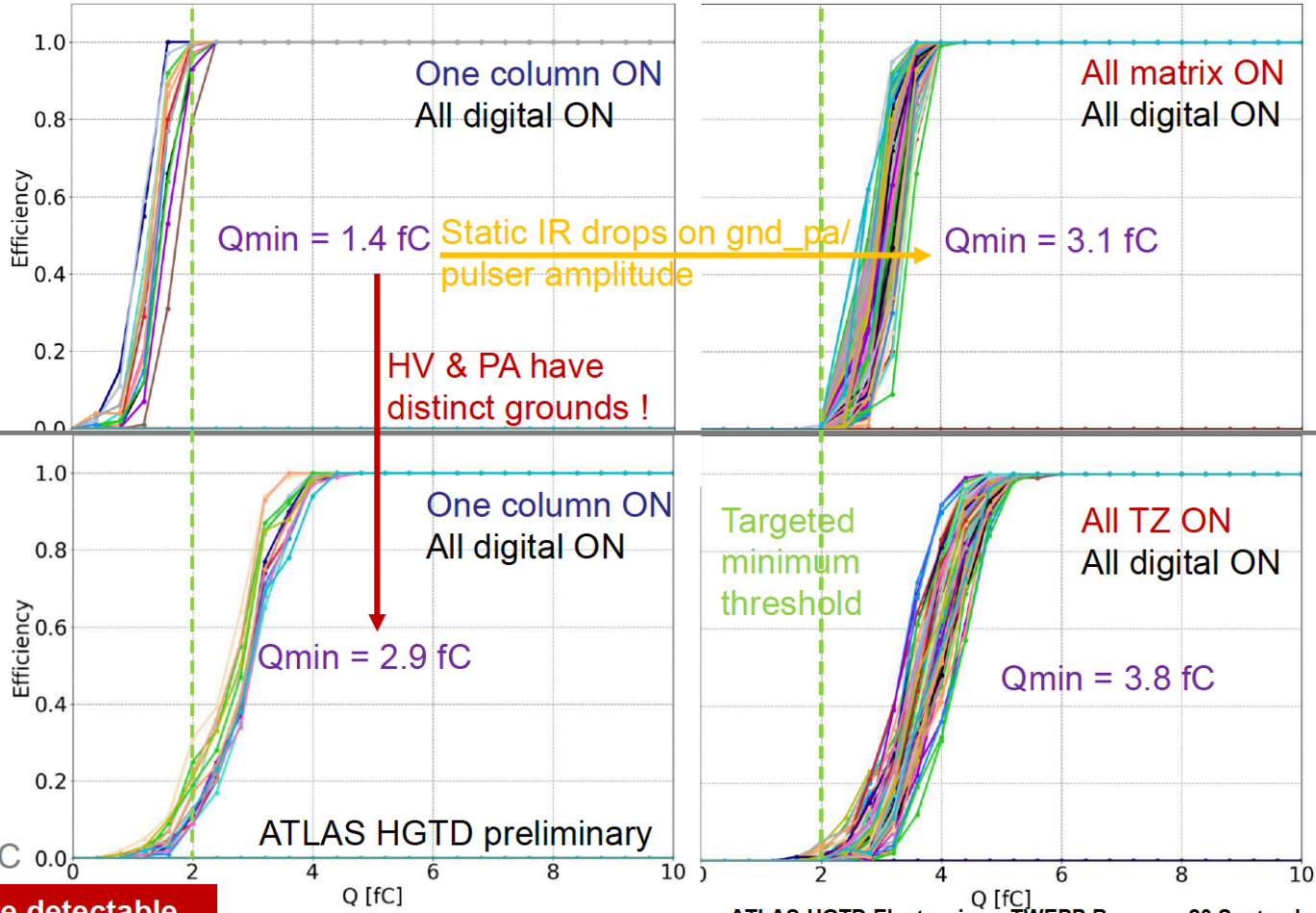
Thanks for listening!

HGTD Production Chain Plan



What is the minimum charge detectable ?

ASIC alone
Irradiated up to 200 Mrad
(B7)



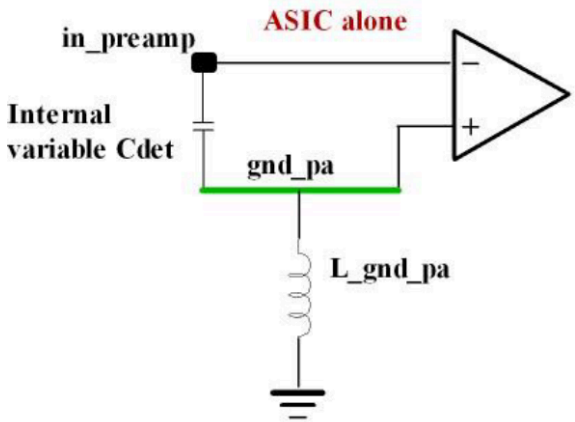
ASIC + LGAD
(B16)

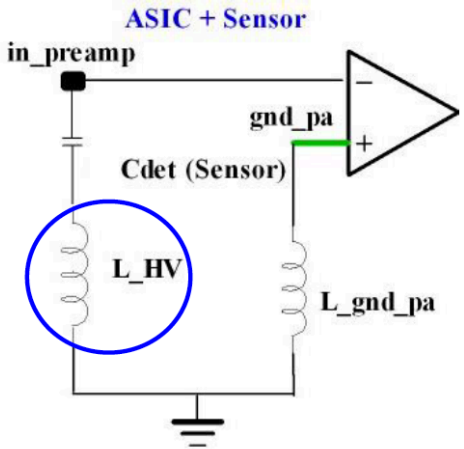
(Median at 50%)

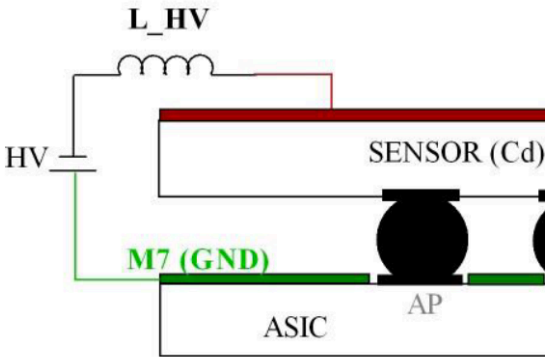
Transimpedance
preamplifier results
Thresholds aligned at 3.2 fC

Limits of the minimum charge detectable

One channel







Noise on analog gnd amplified x1
"common mode"

ASIC alone = favourable situation

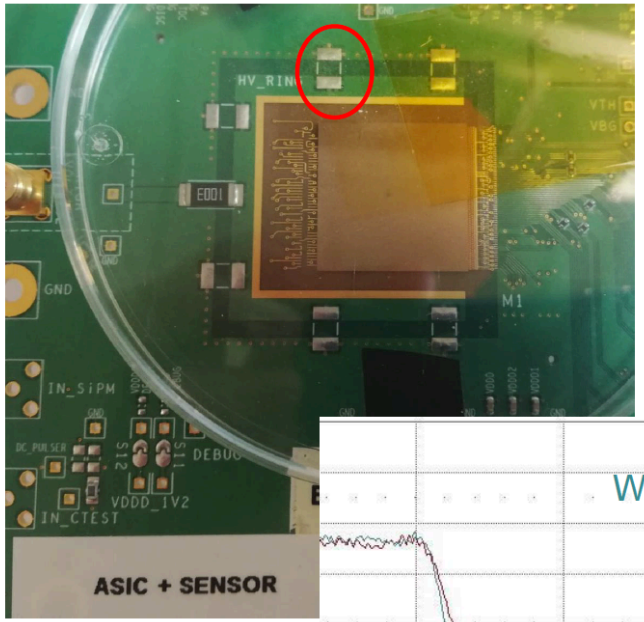
Can this parasitic inductance be hidden from the preamplifier ?

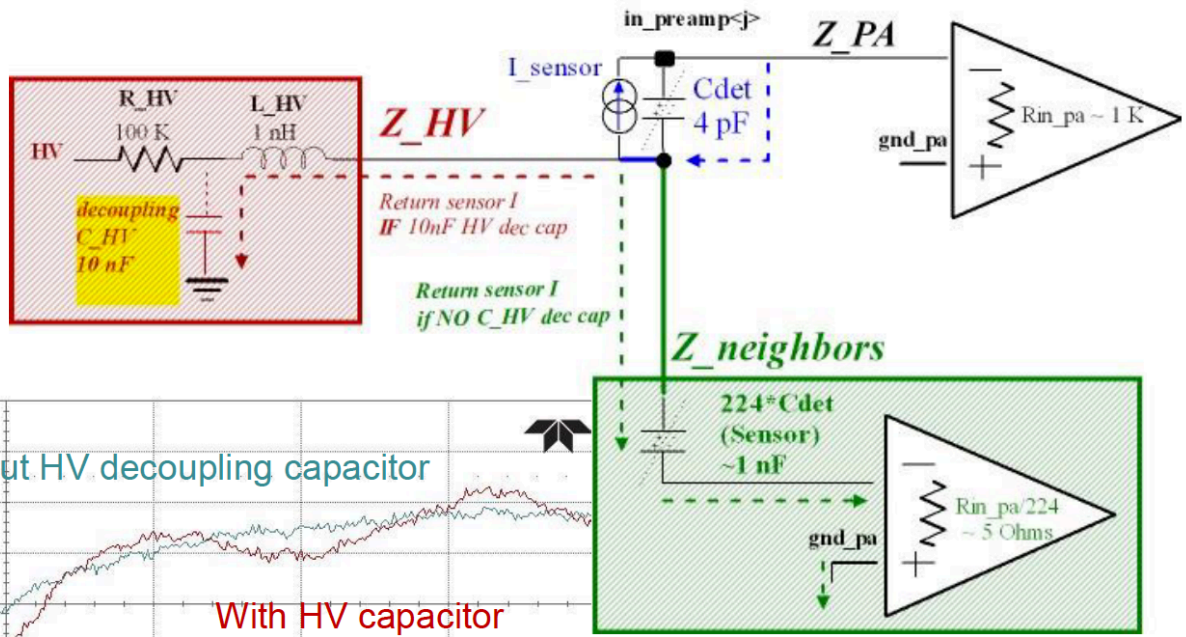
Noise on gnd_pa amplified x20
"differential mode"

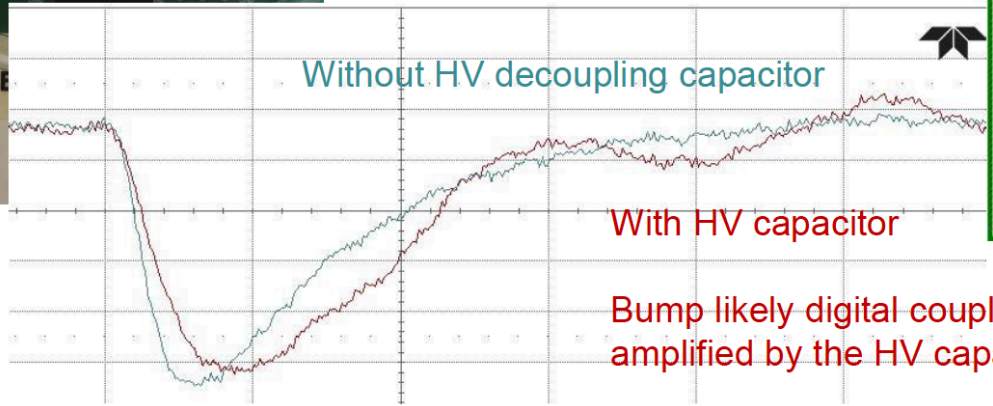
Digital noise injected on the preamplifier ground gets amplified only when the impedance between the detector capacitance and the non-inverting preamplifier input is not zero : when the sensor is connected !

Effect of HV decoupling : where is the AC current flowing back to ground ?

10 nF HV decoupling capacitor adds 50% more noise on a TZ output.



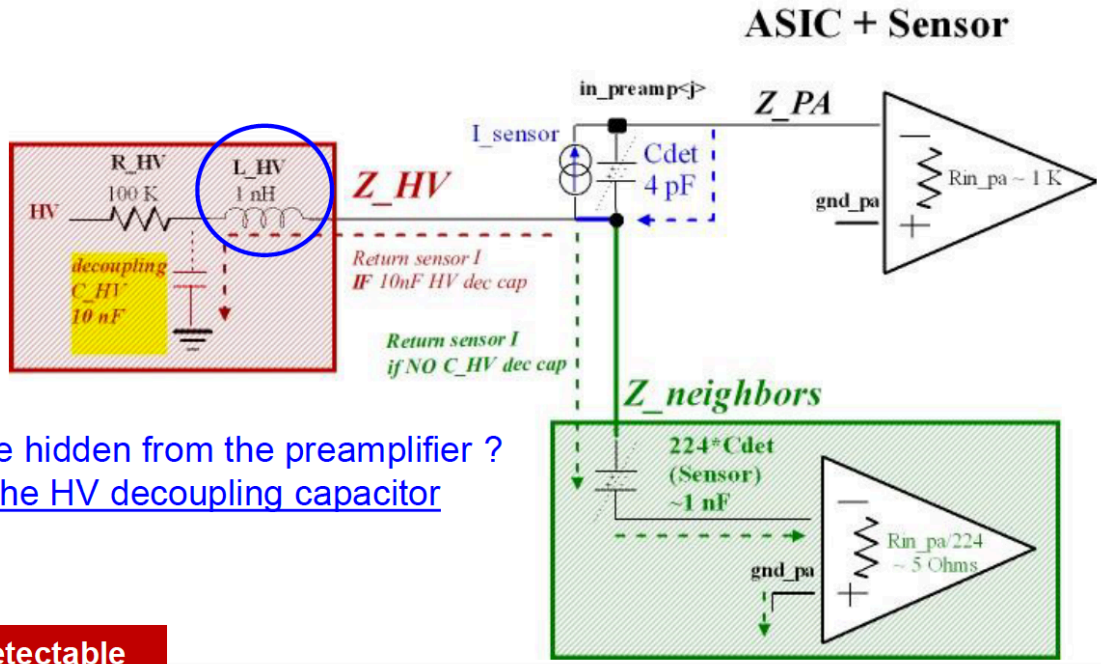




Bump likely digital coupling inside the asic amplified by the HV capacitor

HV impedance (resistance/inductance) is very different for 5x5 and 15x15 sensor

- For small sensor, high impedance leads to deformed signals => the smallest L, the better !
- For large sensor, the low impedance is no longer required as « spectator channels » ensure a low impedance current return
- Higher HV impedance (>100 Ohm) minimizes the gain on gnd_pa => better digital noise



Can this parasitic inductance be hidden from the preamplifier ?
On altiroc2 : yes, by removing the HV decoupling capacitor