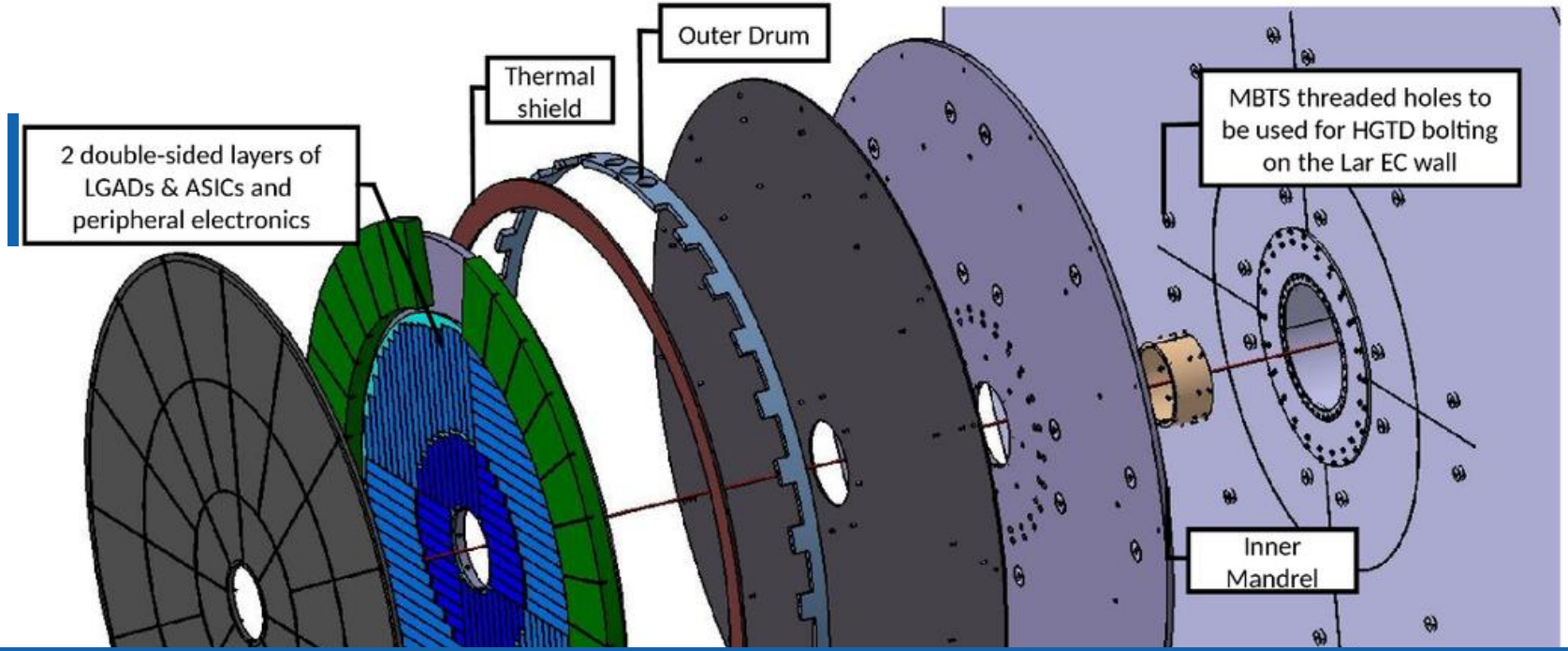


ATLAS Upgrade: HGTD

LIP

ATLAS EXPERIMENT

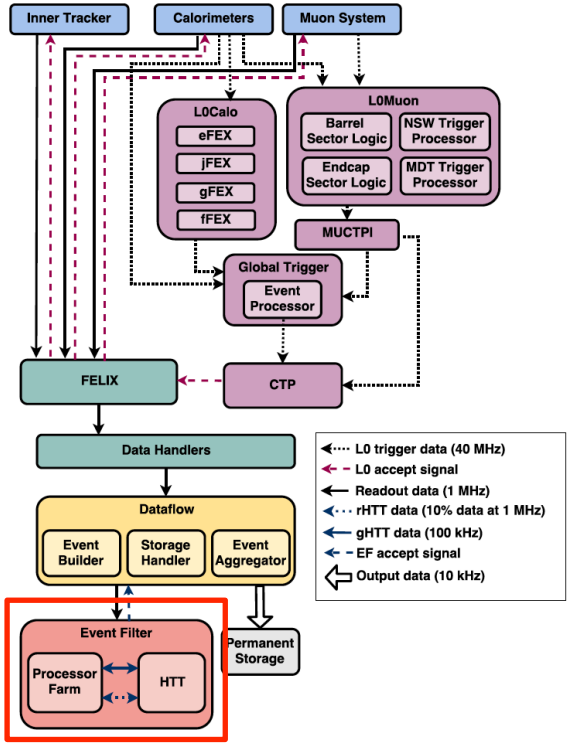
HTT electronics and software

- Hardware tracking co-processor for the trigger:
  - Abandoned by ATLAS in favour of a solution based on software+commodity hardware

- Contributions from LIP:
  - HTT fast simulation; studies of tracking performance – PHD Qualif. Task
  - Alternative tracking algorithm (Hough transform) – MSc thesis
  - Development of TP network interface – only started; TP prototype received late
  - Didn't get here: production of RTM board and DCS
  - Team: 1 academic, 2 engineers, 1 PhD student, 1 MSc student

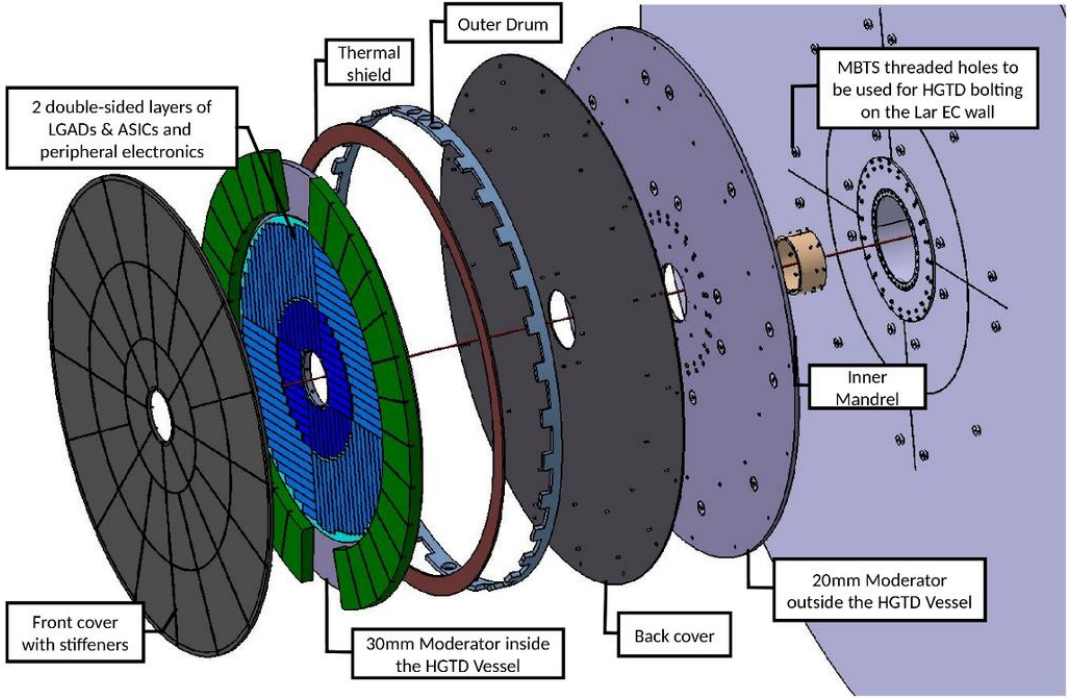






High Granularity Timing Detector

- Two detector wheels at ±3.5 m from IP
- 7 m^2 area, covering region of $2.4<|\eta|<4$
- 8032 LGAD modules of 20×20 mm^2
- Pixel pitch of 1.3×1.3mm^2
- Time resolution 30 – 50 ps / track
- Aims to improve pileup rejection and luminosity measurement



HGTD High Voltage Patch Panels

Aim was developing HV patch panels for CERN group:

- 16 patch panel boxes located around the calorimeter
  - Routing of High Voltage to HGTD detector and filtering out AC noise
- Collaborating with Detector Lab. (Coimbra)
  - Luis Lopes; Orlando Cunha
  - Proposed design and presented in Electronics meetings
  - Built and tested prototype
- Now contributing to Specifications Review (SPR) document

- **Proposal to HGTD**: produce patch panels ourselves at LIP as in-kind contribution – 85 kEUR



ATLAS project

Technical Specification of the High Voltage System

ATLAS Project Document	*Institute Document No. CERN*	*Created:*	*Page:* ***1 of 31***
		Modified:	*Rev. No.:* ***1.0***

HGTD Electronics:

Specification of the High Voltage System

Abstract

This document describes the specifications for the HGTD HV voltage supply system.

Detector Control System

- HGTD DCS design
  - Filipe Martins contributed to DCS Specifications Review
  - Helena interested in taking part – tbd how
  - Filipe working on alternative data transfer scheme following panel recommendations – data path separate from FELIX
- FELIX firmware in collaboration with eCRLab:
  - Part of DCS data to be transferred through FELIX
  - Rui Fernandez to start contributing to firmware
  - Next steps depend on investigation by Filipe and on system decision – alternative means possible MoU contribution
- **Proposal to HGTD**: involvement in HV DCS with person power




HGTD DCS Requirements Document

ATLAS Doc.: AT2-G-ES-0013
EDMS Id: 2648566

ATLAS EXPERIMENT

CERN

ATLAS Phase-II Upgrade Project

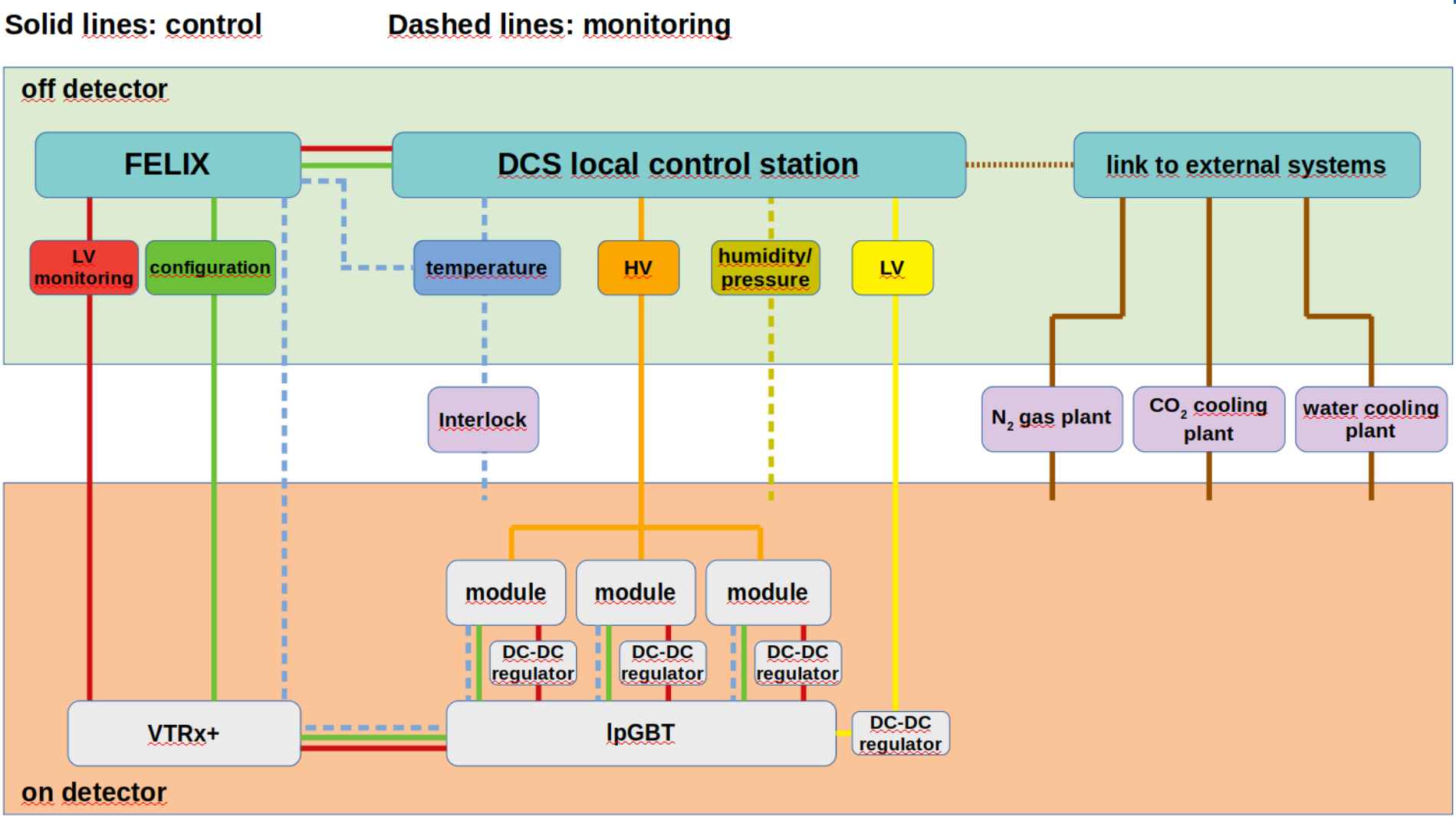
HGTD DCS and Interlock: Requirements Document for HL-LHC

Abstract

This document describes the specifications for the environmental monitoring, the Detector Control System (DCS), and the Interlock system for the High Granularity Timing Detector (HGTD) to be installed in ATLAS (A Toroidal LHC ApparatuS) for Run 4.

HGTD DCS Requirements Document	
ATLAS Doc:	AT2-G-ES-0013
EDMS Id:	2648566
EDMS Url:	https://edms.cern.ch/document/2648566/1
Version:	1.0
Created:	June 2, 2021
Last modified:	January 12, 2022

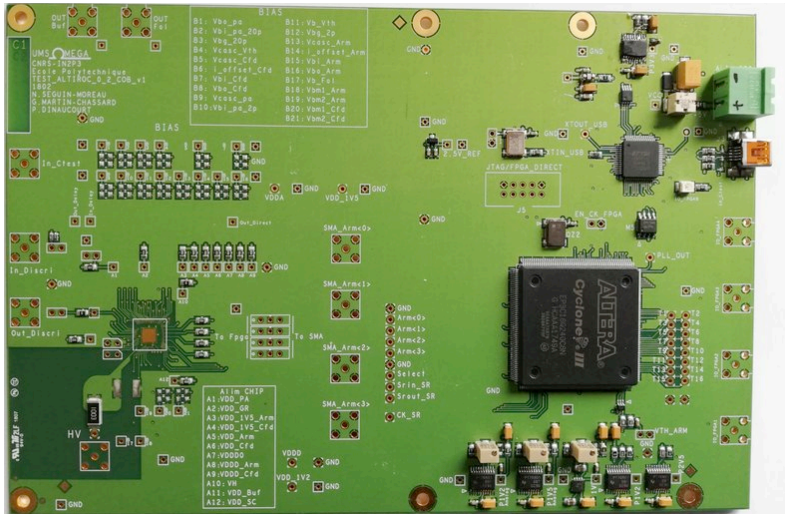
Prepared by:	Checked by:	Approved by:
K. Gritsay, B. Lund-Jensen, S. Malyukov, J. Strandberg, M. Wu	S. Grinstein, F. Martins P. Teterin, J. Zhang	J. Guimarães da Costa

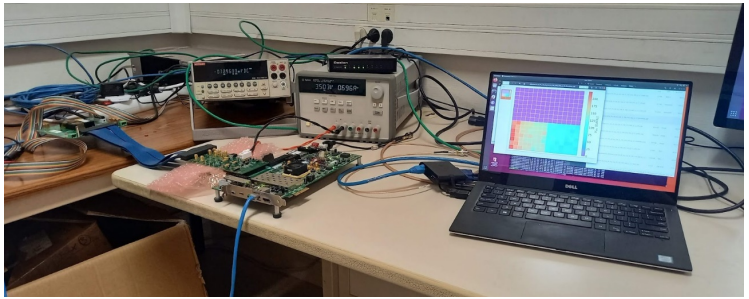

Solid lines: control
Dashed lines: monitoring
off detector
FELIX
DCS local control station
link to external systems
LV monitoring
configuration
temperature
HV
humidity/ pressure
LV
Interlock
N2 gas plant
CO2 cooling plant
water cooling plant
module
module
module
DC-DC regulator
DC-DC regulator
DC-DC regulator
VTRx+
lpGBT
DC-DC regulator
on detector

Altiroc ASIC

- Getting involved with testing Altiroc v.2
  - In collaboration with eCRLab
  - 6 institutes already involved – but interest in gaining experience with this
  - Rui Fernandez involved, with support from Miguel Ferreira and Pedro Assis
- In contact with Omega lab. to obtain material, to install a test setup at LIP

- **Proposal to HGTD**: involvement in Atiroc development with person power (little cost)





Impact and Upgrade MoU

HTT: MoU share of ~600 kEUR
HGTD project:

- Only ~112 kEUR CORE funds missing, in HGTD DAQ (some 6 months ago)
- Little existing experience in DCS – possible important impact from group
- Developing challenging Altiroc front-end ASIC – technological interest
- Patch panels – way into project and possible group responsability – 85 kEUR
- Ideal: pay people from MoU – maybe easier on TDAQ tasks

Other areas:

- Interlocks:
  - Mostly temperature sensors connected to Interlock Matrix Crate (IMC) located in USA15, similarly to Itk
  - Possible LIP involvement: interface to ATLAS interlock system (15 kEUR)
- Performance studies:
  - Suitable for student qualification tasks

Thanks!

Acknowledgments

REPÚBLICA PORTUGUESA

FCT Fundação para a Ciência e a Tecnologia

Possible areas of involvement

DCS:
- Software involvement – much expertise in the group

Interlocks:
- Mostly temperature sensors connected to Interlock Matrix Crate (IMC) located in USA15, similarly to ITk

DAQ, Lumi, timing?:
- Firmware (& hardware?) – opportunity for collaboration with eCRLab and João Varela/CMS

Performance studies:
- Suitable for student qualification tasks

112 kCHF CORE funds missing (TDAQ)

Backup