ATLAS Upgrade

Jornadas do LIP

Universidade de Coimbra – 8 July 2022

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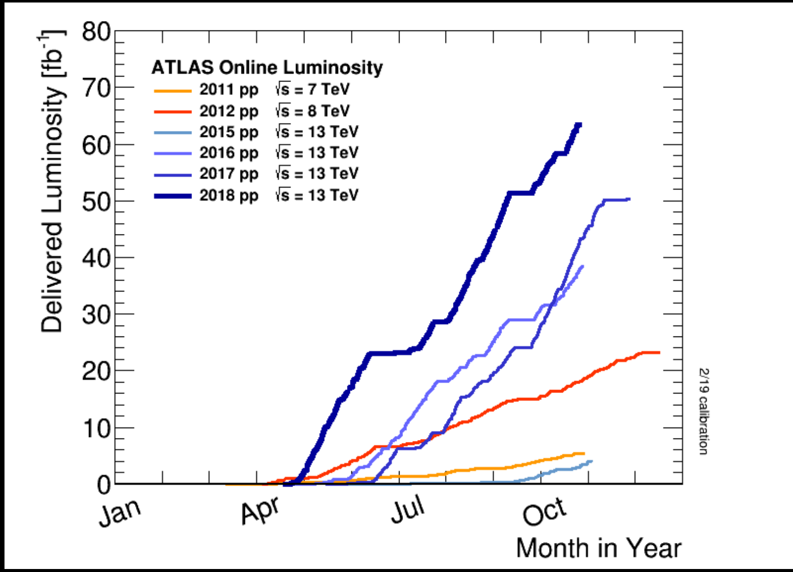
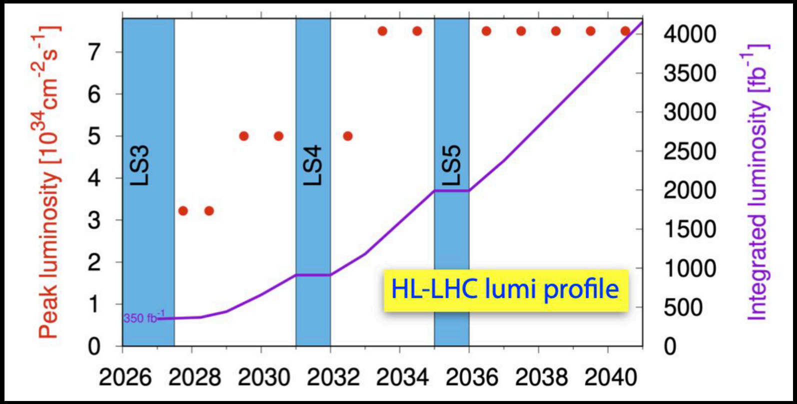
Universidade de Coimbra / LIP

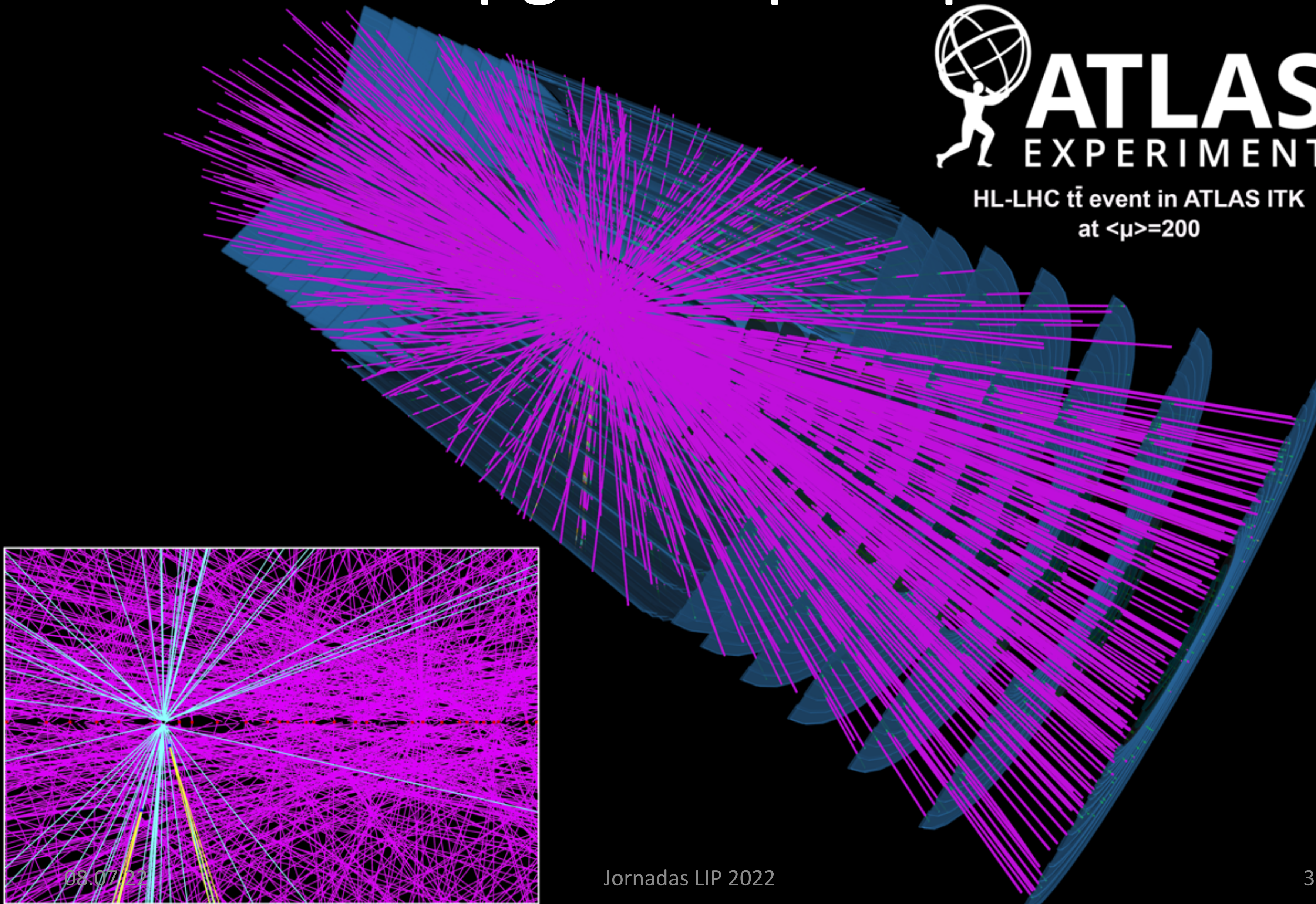
ATLAS Upgrade: Motivation for HL-LHC



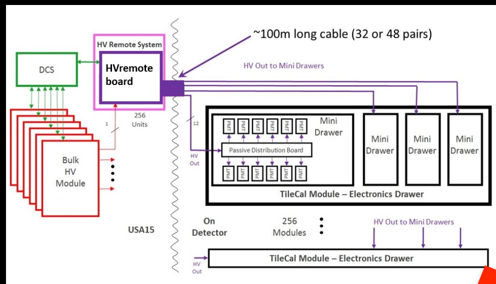


- High-Luminosity!
  - Statistical uncertainty depends on √L
- So far collected ≈150 fb^{-1} of data at √s=7, 8 and 13 TeV
  - Less than 5% of final
  - Resulted in 1039 published papers
  - Goal is to collect up to 4000 fb^{-1} until end of LHC
- => Increase instantaneous luminosity!
- Downside: PILEUP
  - Affects experiment performance
  - Average ≈30 so far
  - Expect up to 200 in HL-LHC

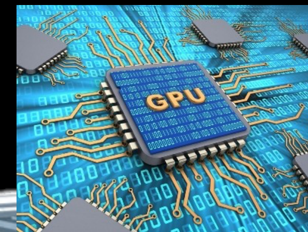
ATLAS Upgrade: pileup = 200



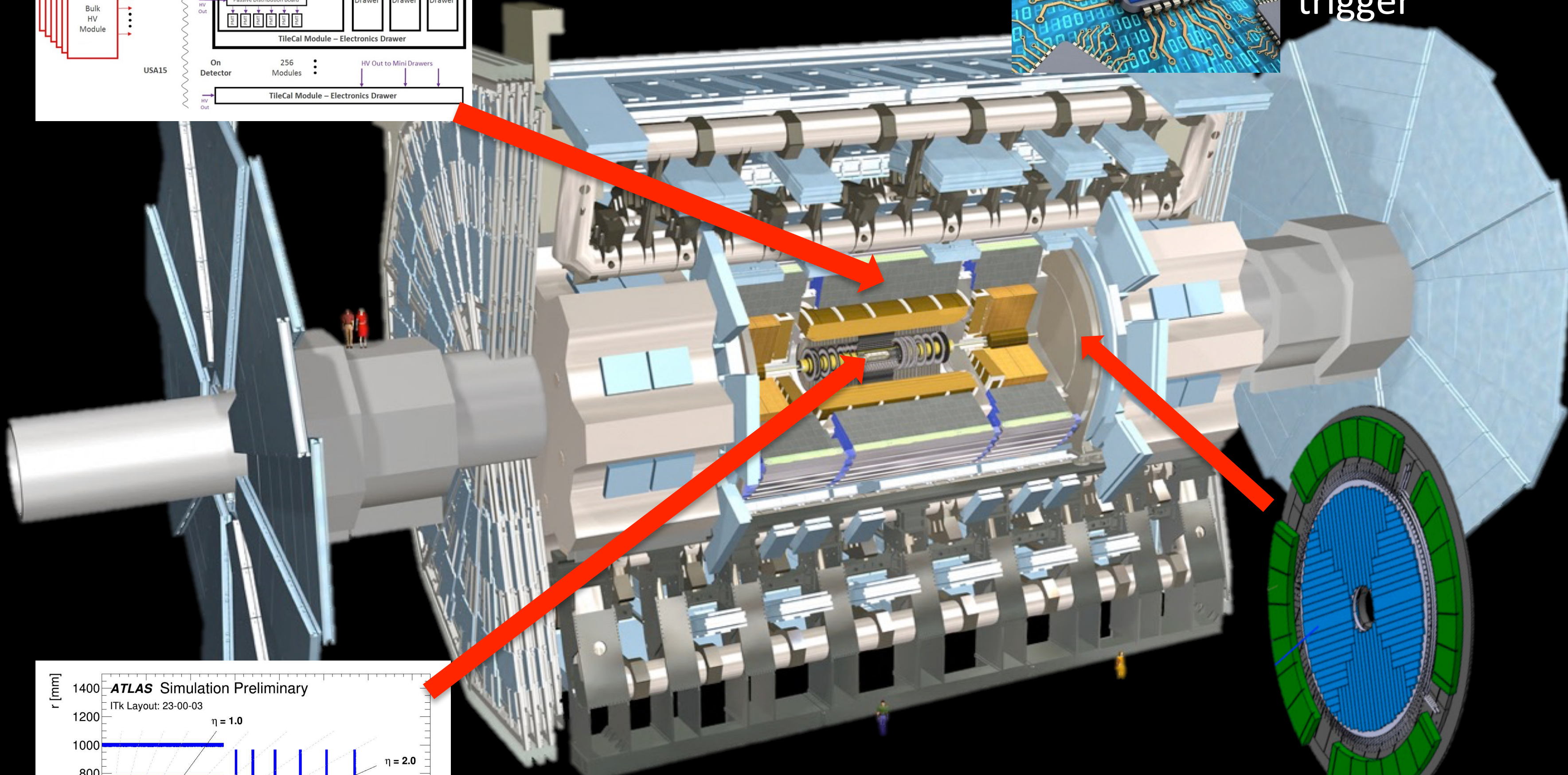
ATLAS Upgrade @ LIP

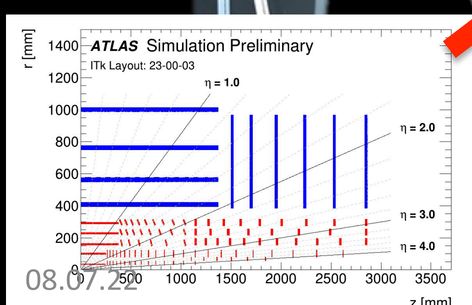


New Tile Calorimeter High-Voltage system



R&D on hardware acceleration for trigger

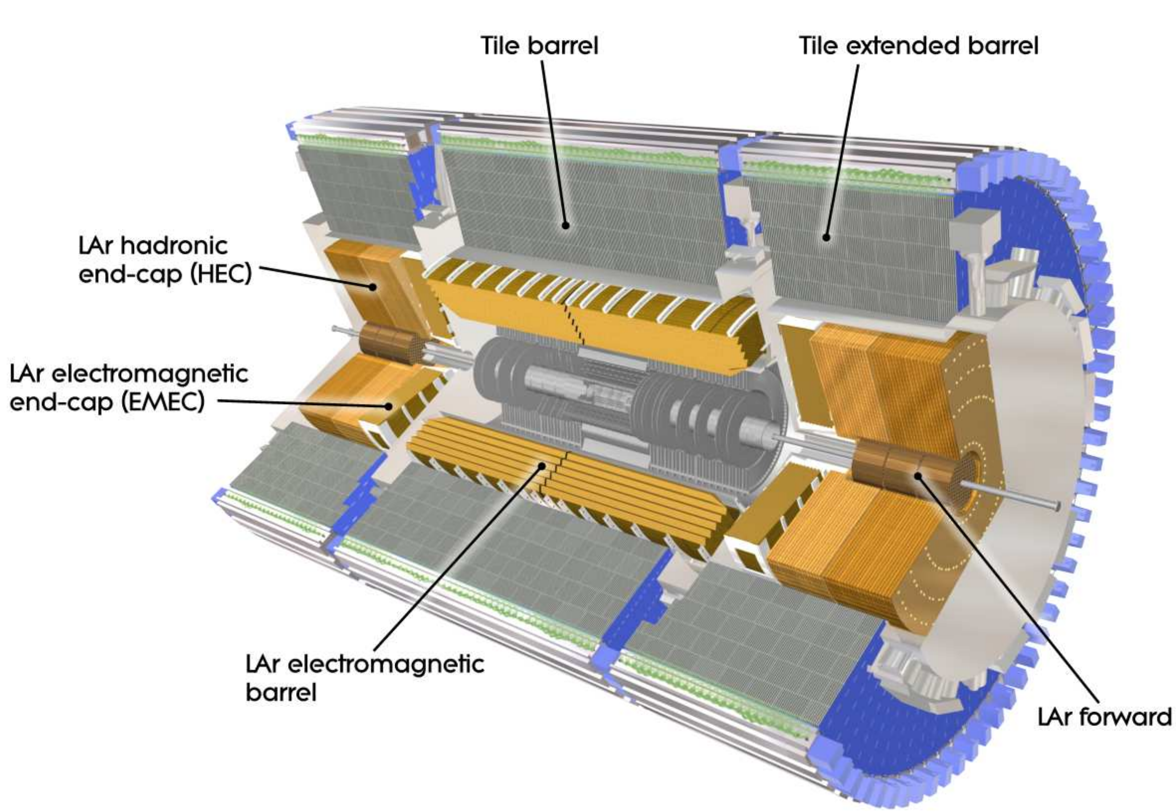


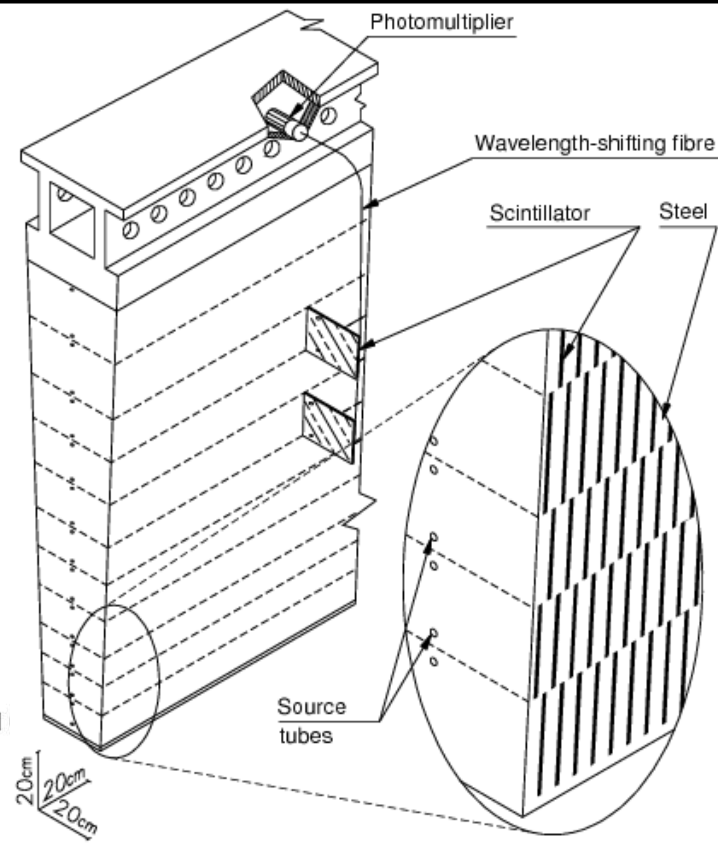


Track reconstruction for New Inner Tracker (ITk)

High Granularity Timing Detector (30ps/track)

ATLAS TileCal Upgrade





HV System: Agostinho Gomes, Guiomar Evans, Luís Gurriana, Filipe Martins, José Augusto, Rui Fernandez, Pedro Assis, Miguel Ferreira, José Carlos Nogueira (collaboration with eCRLab)

Optics Robustness: Rute Pedro, Beatriz Pereira

TileCal High-Voltage System

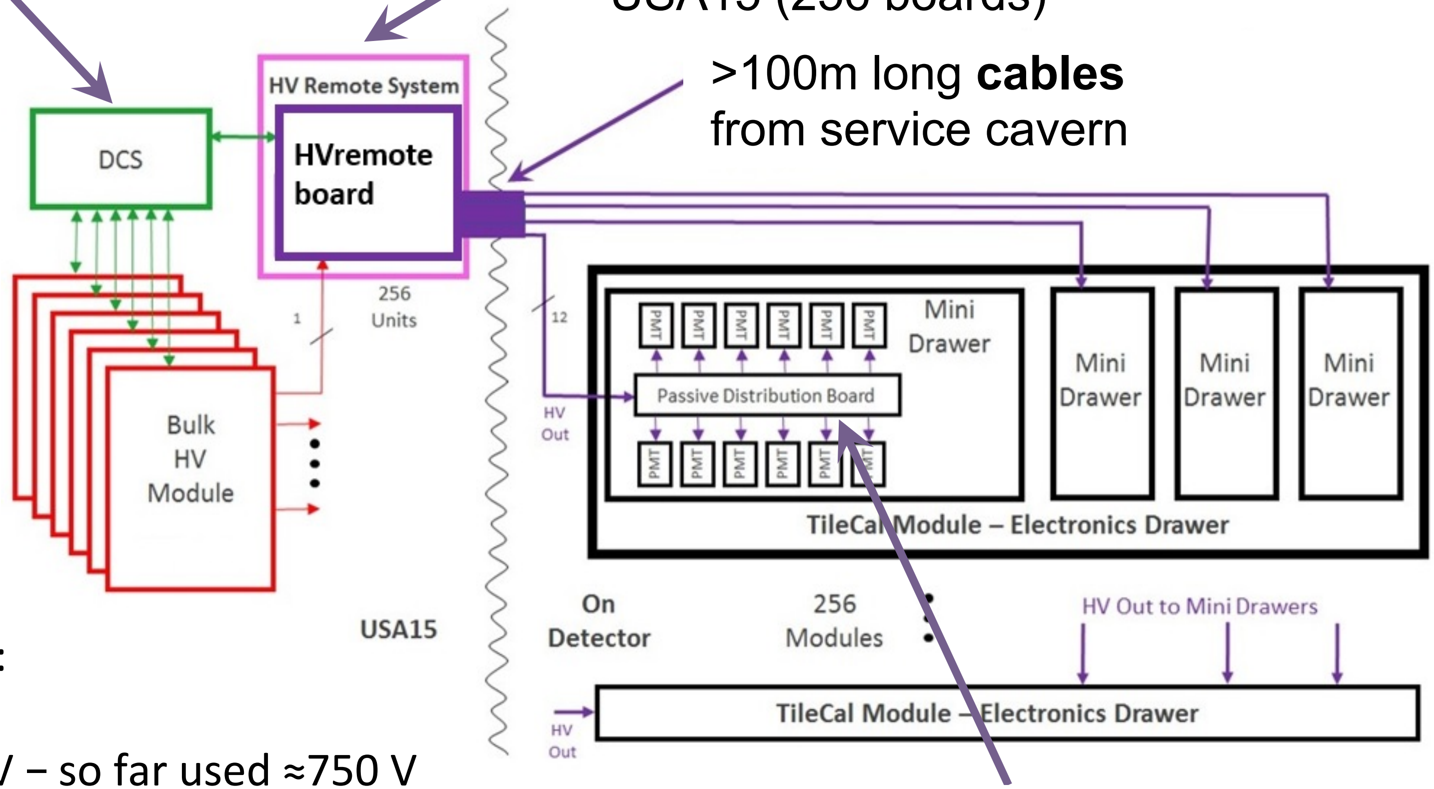
DCS system: SoC board for High Voltage monitoring & control

HVSupplies provide primary High Voltage (256 boards)

16 crates in service cavern

HVRemote boards - Regulation and control system off detector at USA15 (256 boards)

>100m long **cables** from service cavern



System parameters:

10000 PMTs

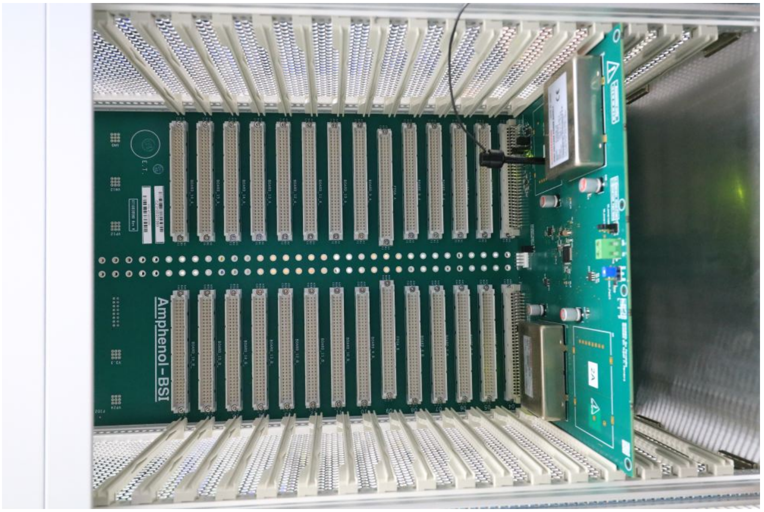
High Voltage < 950 V – so far used ≈750 V

Individual currents < 400 μA

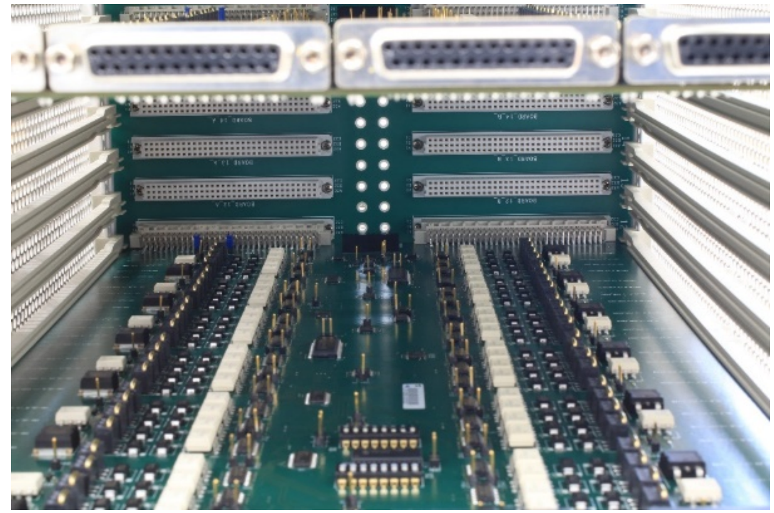
High Voltage stability < 0.5 V rms

HVBus – passive distribution board distributes HV to PMTs (1024 boards)

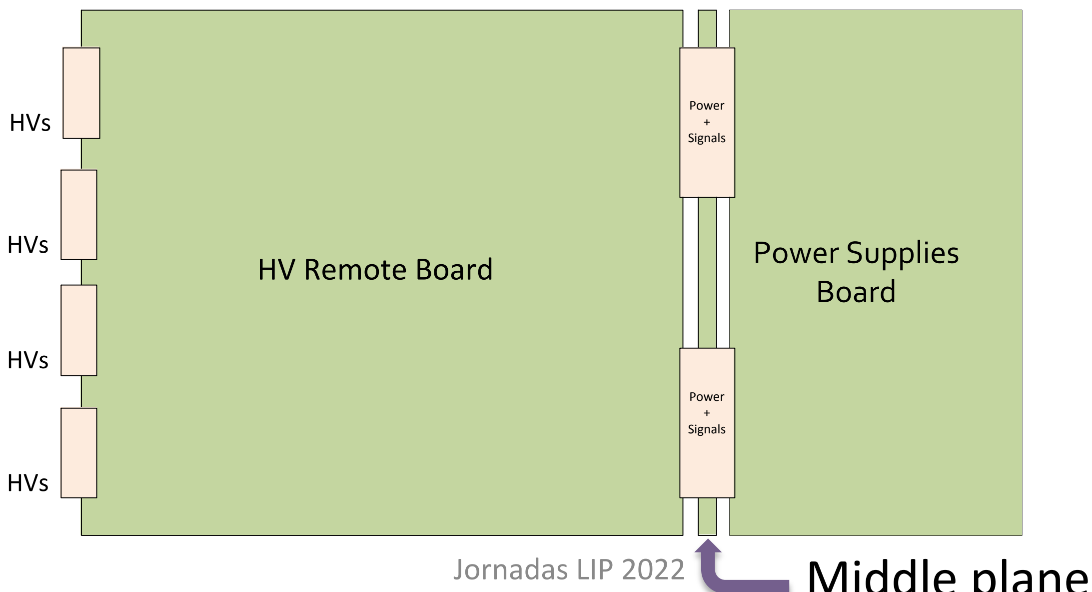
High Voltage System Components



Front of crate: **HVSupplies** board

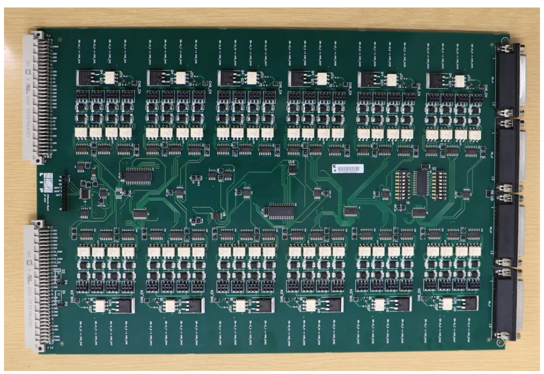


Back of crate: **HVRemote** boards

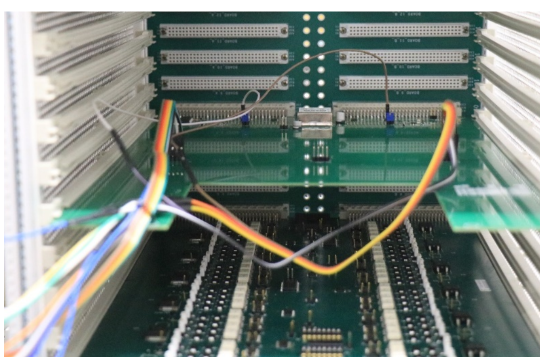


High Voltage System Components

- **HVSupplies**:
- DC-DC converters to produce primary HV
- Connects with the ATLAS Detector Safety System Designed by eCRLab
- First prototypes **successfully tested** and a new design finished for production



- **HVRemote**:
- Receives 2 primary HV inputs from **HVSupplies**
- Sends 48 individually regulated HV outputs to **HVBus**
  - DACs to set the individual voltages
  - Regulation loops based on optocouplers
  - On/Off available for sets of 4 channels

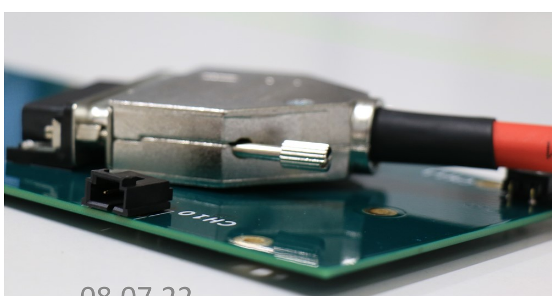


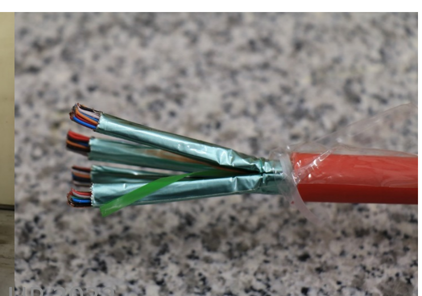
- **HV Control Board**:
- One Zybo Z7 Zynq System-on-Chip (SoC) interface board per crate
- Two SPI buses (one to the HVRemote and other to the power supply boards);
- Tests showed a few bugs, some corrections required

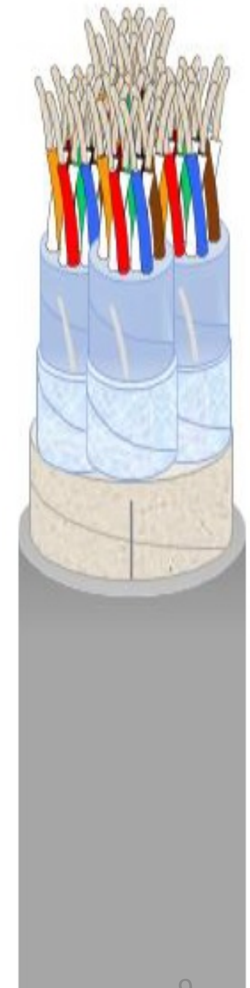
High Voltage Distribution

- **Cables**:
- New 48 wire pairs cable developed in Portugal with General Cable
  - 10000 PMTs => 20000 wires 100 m long
  - > 41 km for final system
  - Wire diameter: 0.4 mm
  - Aluminium/PETP tape screen and drain wire ensures electromagnetic shielding
  - Prototypes produced

- **HVBus**:
- HV bus and short cables for HV distribution produced and being tested



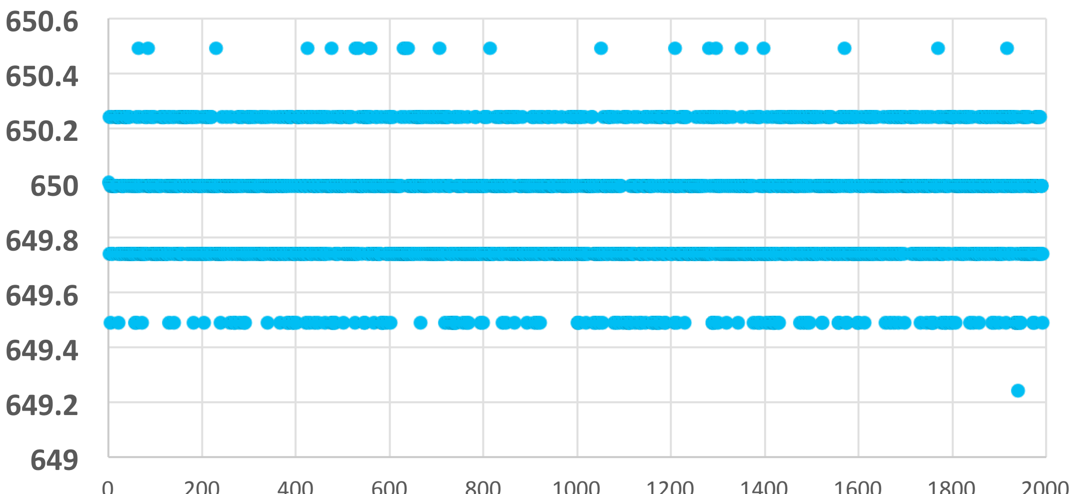


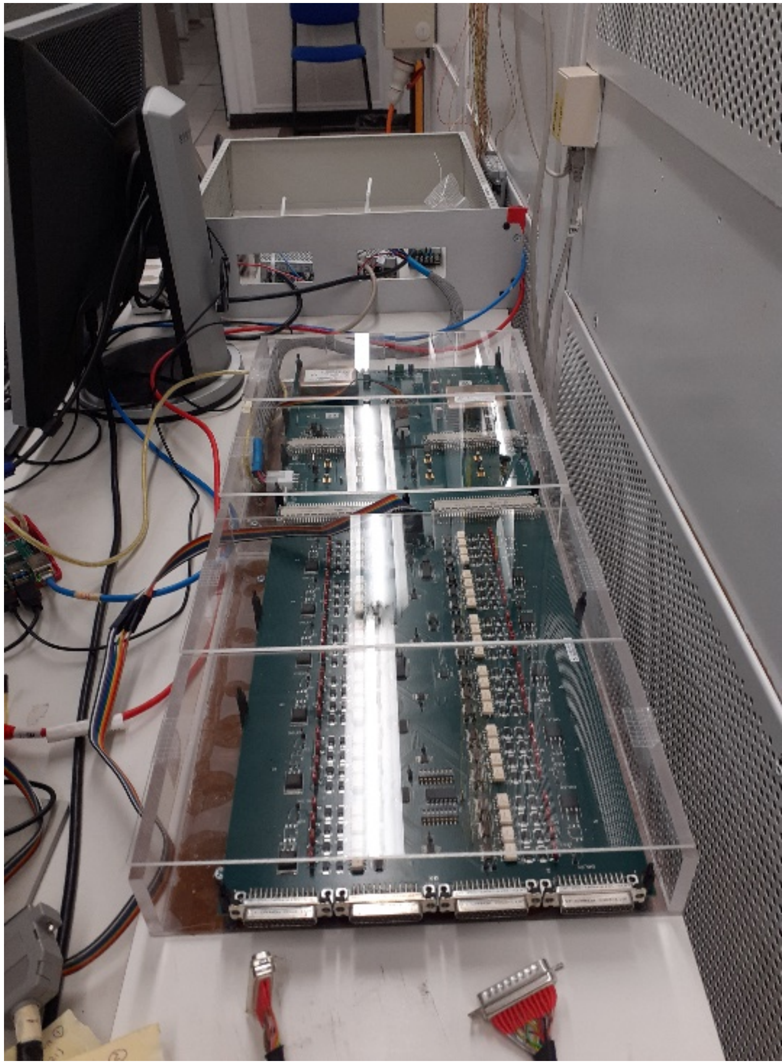


Testing Programme

- **Testbeam**:
  - Tested **HVSupplies** + adapter board + **HVRemote** + **Hvbus** in 2021 and June 2022
  - Will test **Crate** + **SoC interface** + final boards in November 2022

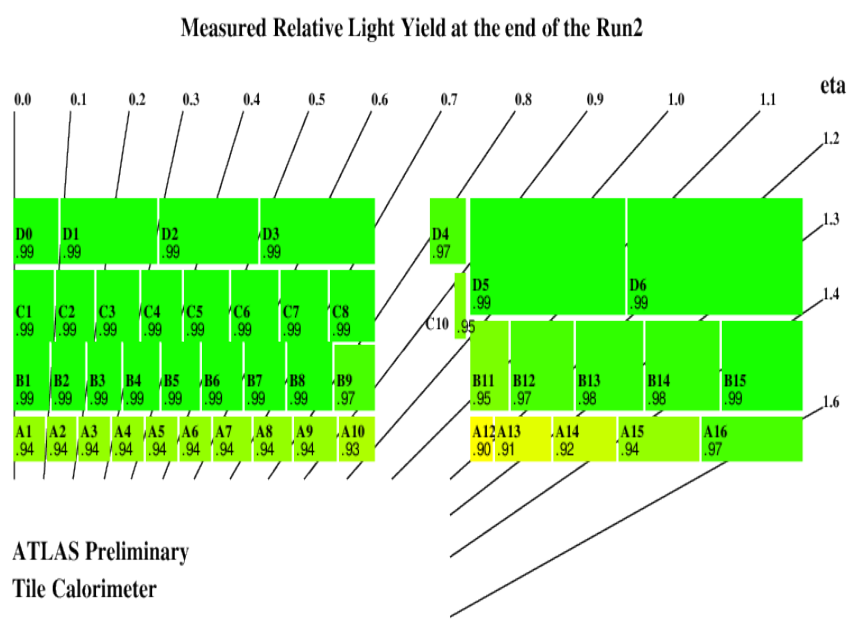
- **Stability** tests:
  - > 5h long tests
  - **rms ≈ 0.21 – 0.23 V**

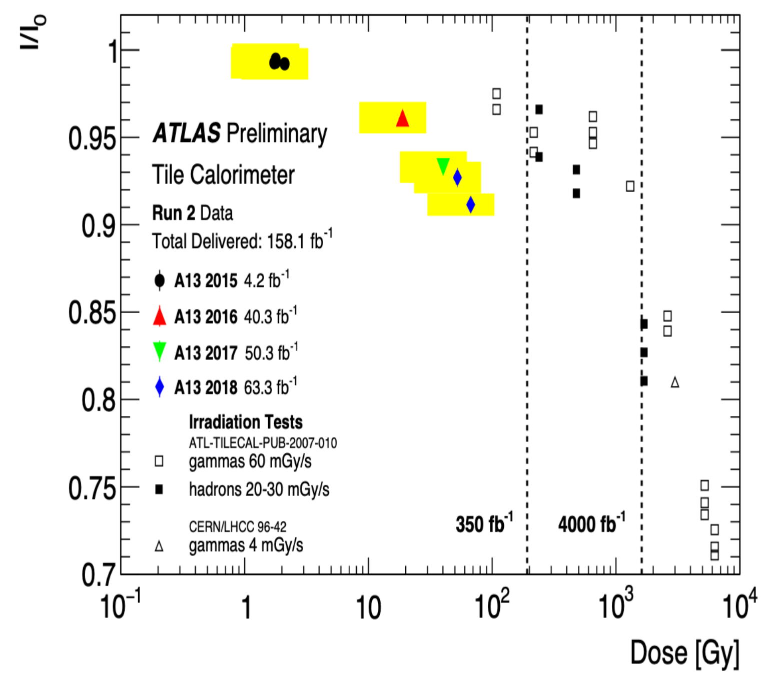




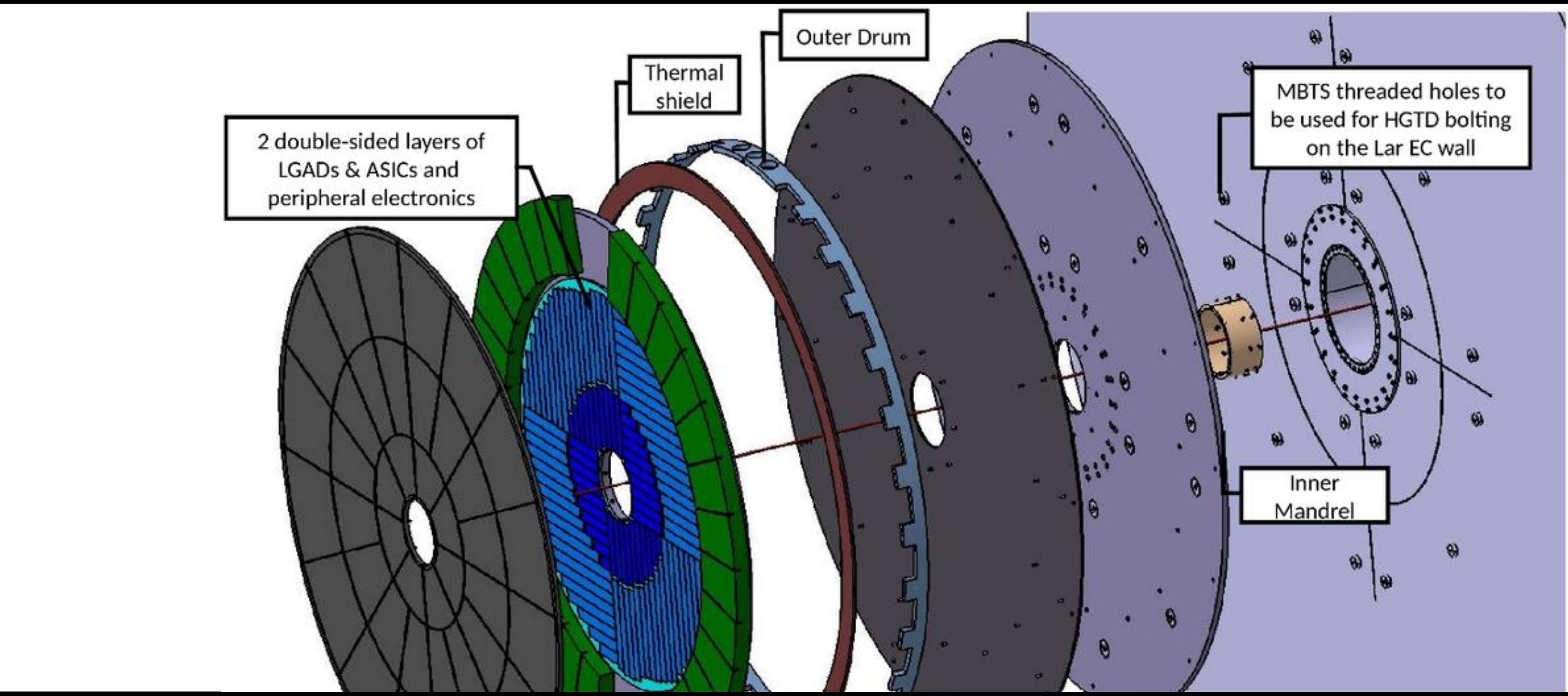
TileCal Optics Robustness for HL-LHC

- The HL-LHC will bring additional radiation exposure and damage to the TileCal scintillators and fibres
- Measured Run 2 light yield from Laser and Cs data
- Modeling the light response as a function of ionising dose
- Cs calibration data at sub-cell level helps to reduce uncertainties due to dose spread within the cell volume (ongoing work)



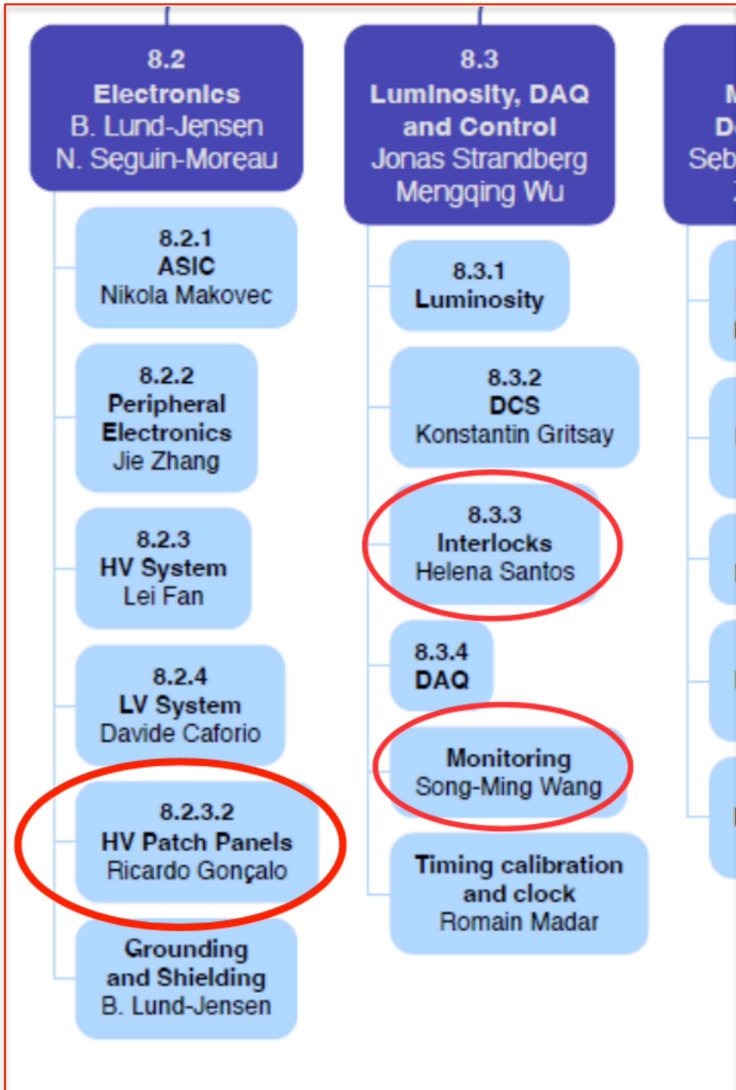


High Granularity Timing Detector

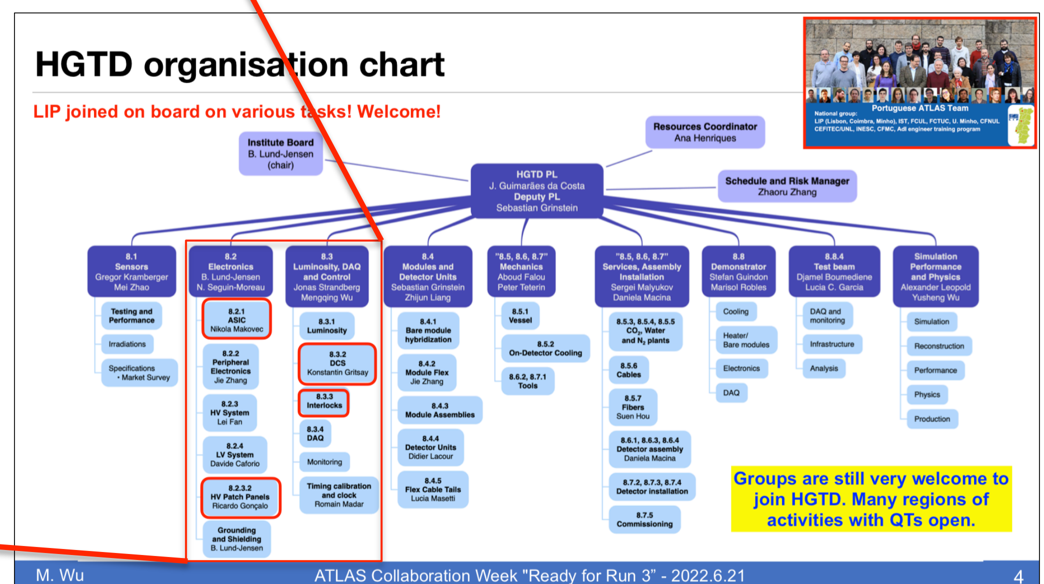


HV System: Luis Lopes, Orlando Cunha, Ricardo Gonçalo – collaboration with Detector Lab
ASIC tests: Rui Fernandez, Pedro Assis, Miguel Ferreira – collaboration with eCRLab
DCS and Interlocks: Filipe Martins, Rui Fernandez, Helena Santos, Guiomar Evans

HGTD @ LIP



- Recent involvement since last year, but significant impact
- Contributing to several areas:
  - **Electronics**: readout ASIC tests, High Voltage filtering
  - **Detector control** and safety **Interlocks**
  - Monitoring
- Other **possibilities** being followed:
  - Cable production in Portuguese industry
  - Mechanical design and production at LIP

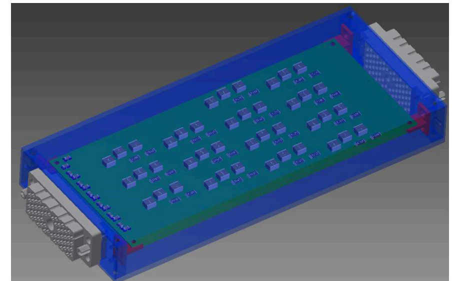
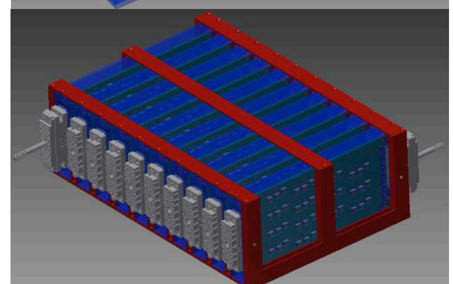
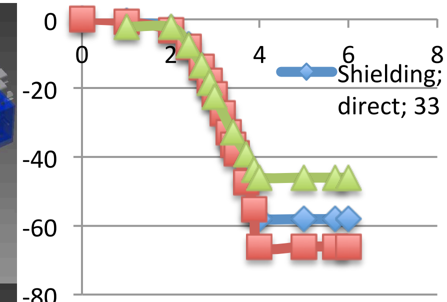


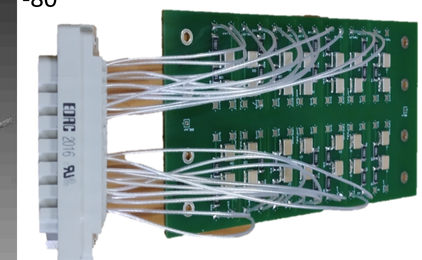
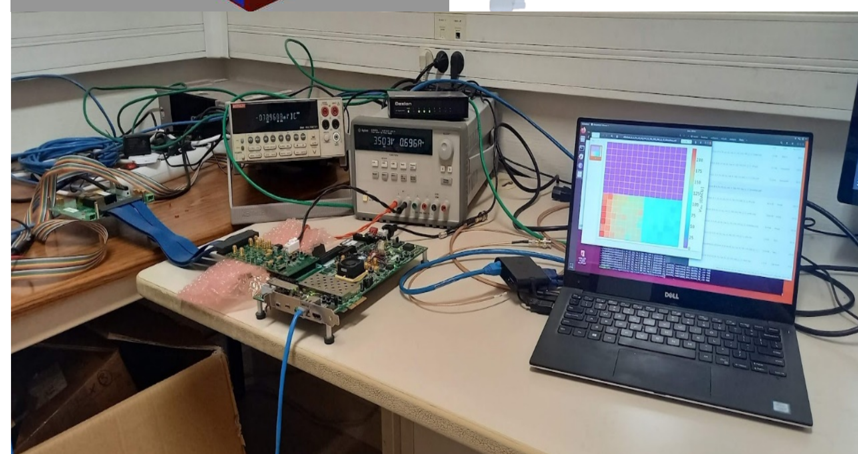
Electronics and High-Voltage

HV patch panels:
- Responsible for producing HV patch panels
- Routing and **filtering** High Voltage to HGTD detector
- Preliminary layout done and prototype tested
- Design being updated after **review**

Cables:
- May also produce HV **cables** (under negotiation)

ALTIROC:
- **ASIC** under development for LGAD readout
- Plan to take part in ASIC **development tests**
- Contact established with developers (OMEGA) and testing infrastructure almost in place

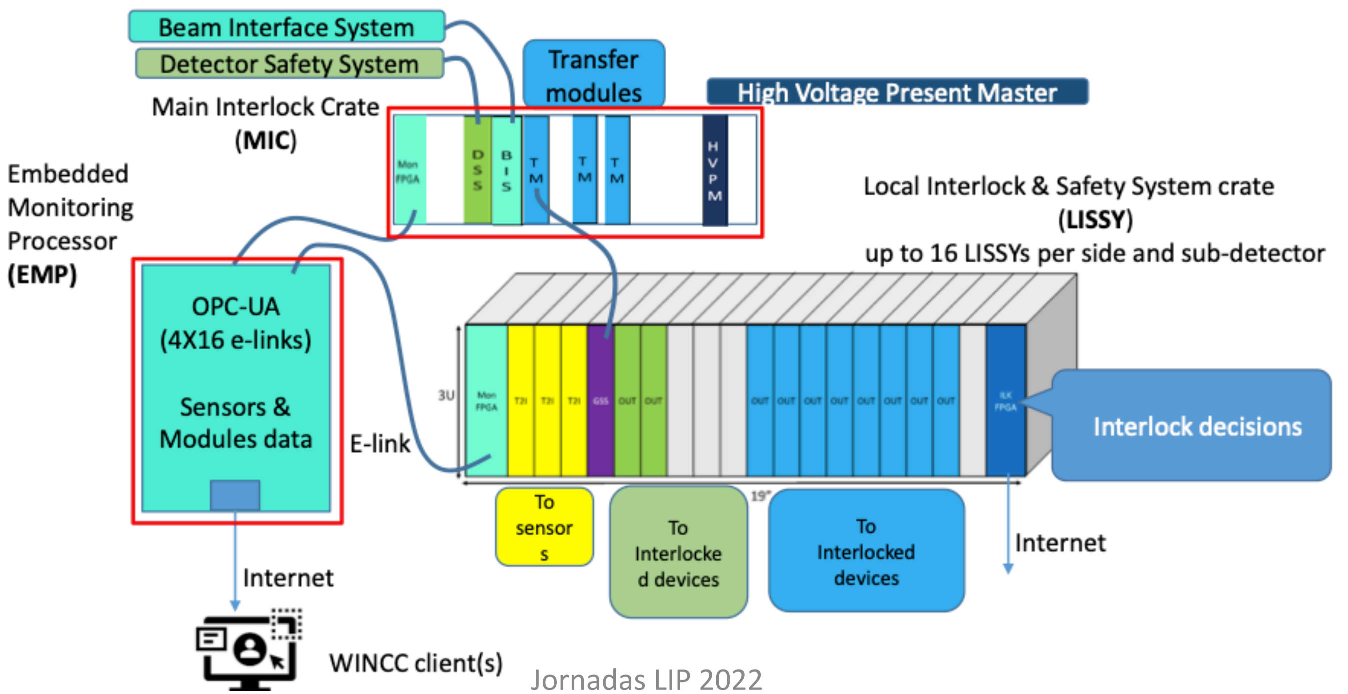




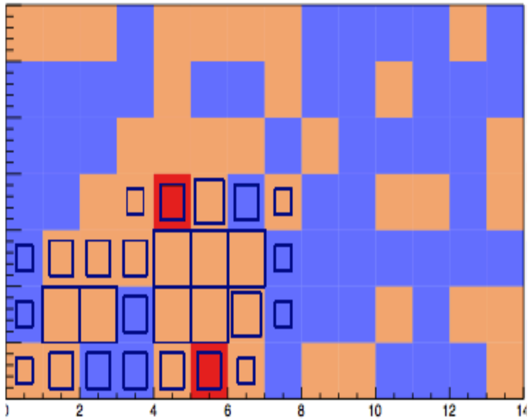

DCS and Interlocks

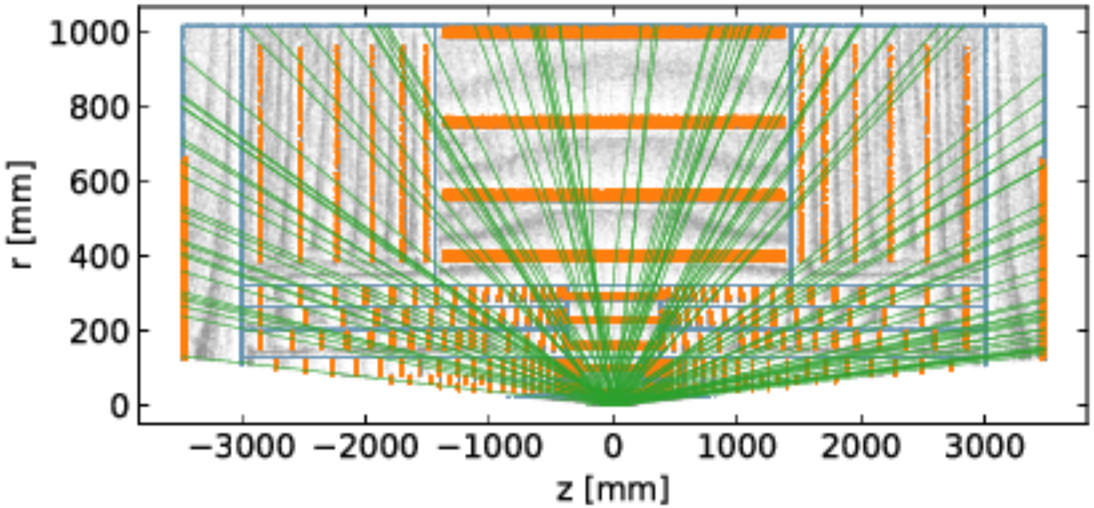
- **Detector Control System (DCS)**:
  - Contributing to DCS architecture definition
  - Readout of DCS environment data through ELMB2 communication board

- **Interlocks** (started recetly):
  - Taking responsability for HGTD Interlocks – mostly will re-use ITk design
    - Likely to produce an interlock module ourselves (HV-Present)



Reconstruction Algorithms for Phase 2

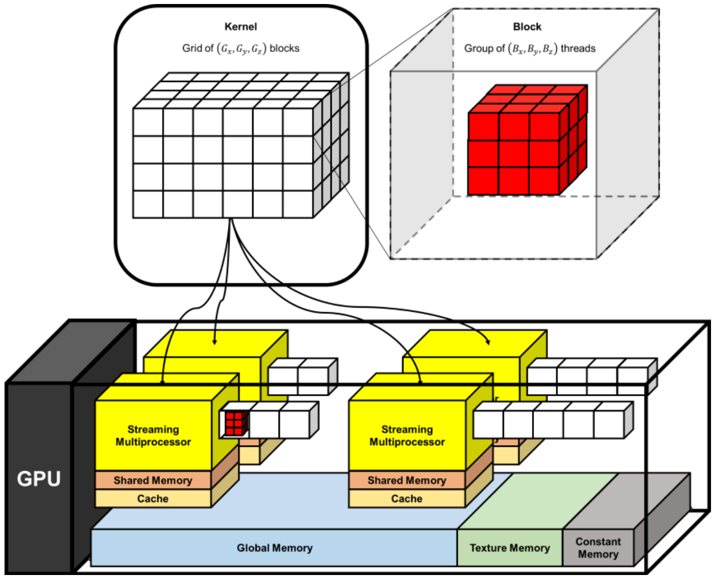


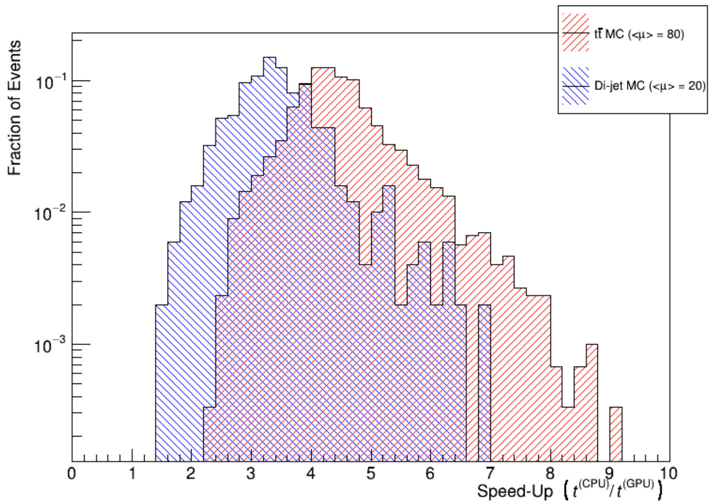


GPUs: Nuno Fernandes, Patricia Conde
Muon trigger: João Gentil
ACTS: Luis Coelho, Noemi Calace, R.goncalo

ATLAS Trigger Upgrades

- **GPU acceleration** to deal with increased event rates
- **GPU-based Topo-Automaton Clustering (TAC)** cellular automaton algorithm
  - Group cells by **signal-to-noise ratio**
  - Important **overhead** from data structure convertion to and from GPU format
- Speed-up:
  - **3.5** (di-jets) to **4.5** (top pairs)
  - < 40% of time: algorithm
  - 50 - 55% of time conversion overhead
  - 10 - 15% of time CPU↔GPU data transfer (TeslaT4andaAMDEPYC7552)

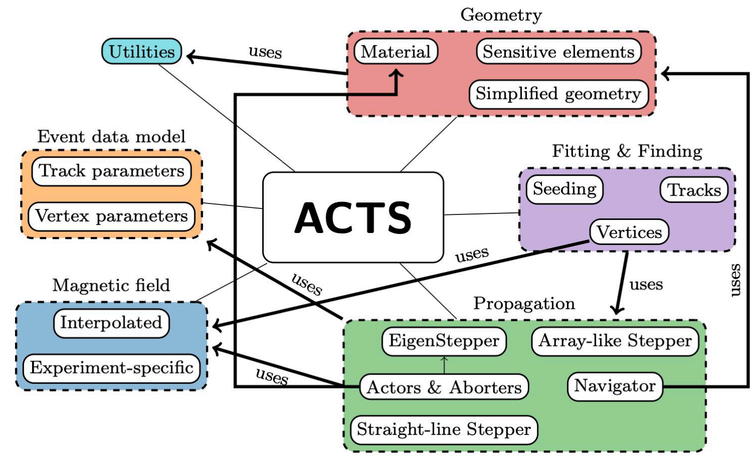




- Also new **Muon trigger**:
  - Using minimum-bias scintillators for fake jet rejection (J.Gentil)

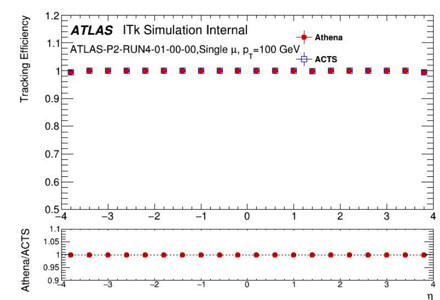
A Common Tracking Software (ACTS)

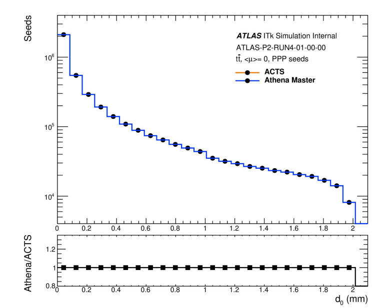
- Tracking of charged particles is one of the the most complex and CPU consuming phases of event reconstruction
- Will become even greater computational challenge during HL-LHC



ACTS:

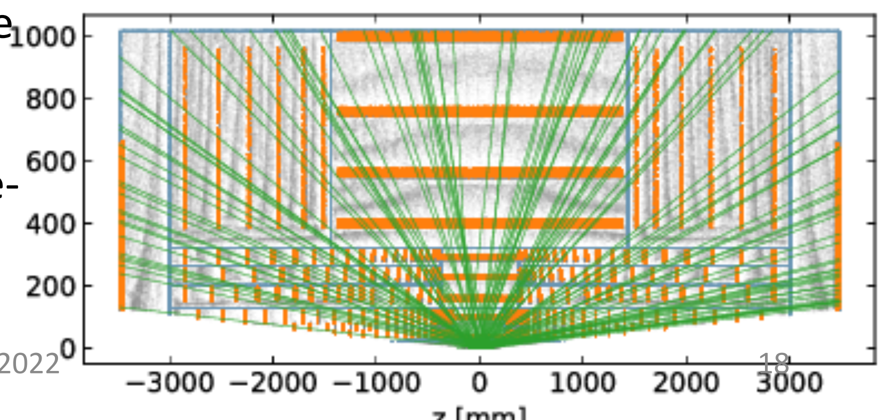
- Experiment-independent toolkit for particle track reconstruction
- Designed for modern computing architectures and multi-threaded event processing





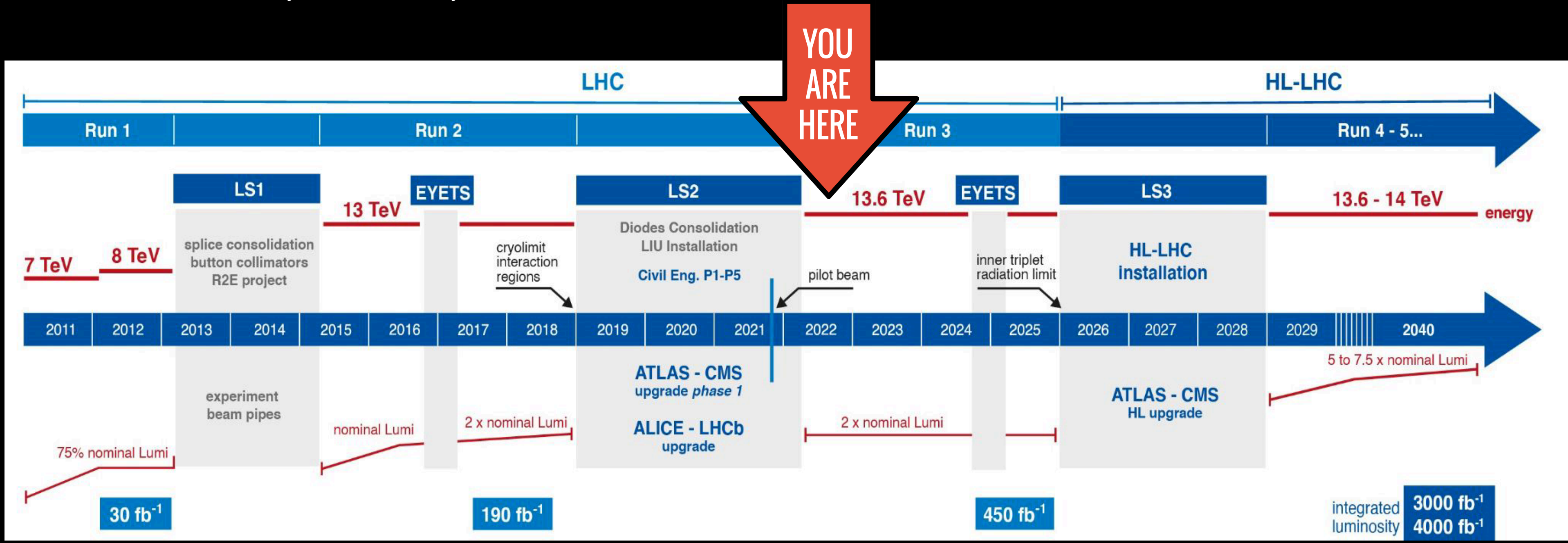
Goal:

- Implement ITk seeding algorithm in ACTS and integrate into standard ATLAS code and validate its performance
- **The Seeding Algorithm**
- Forms track seeds consisting of triplets of space-points (SP) based on geometrical assumptions relative to the interaction point

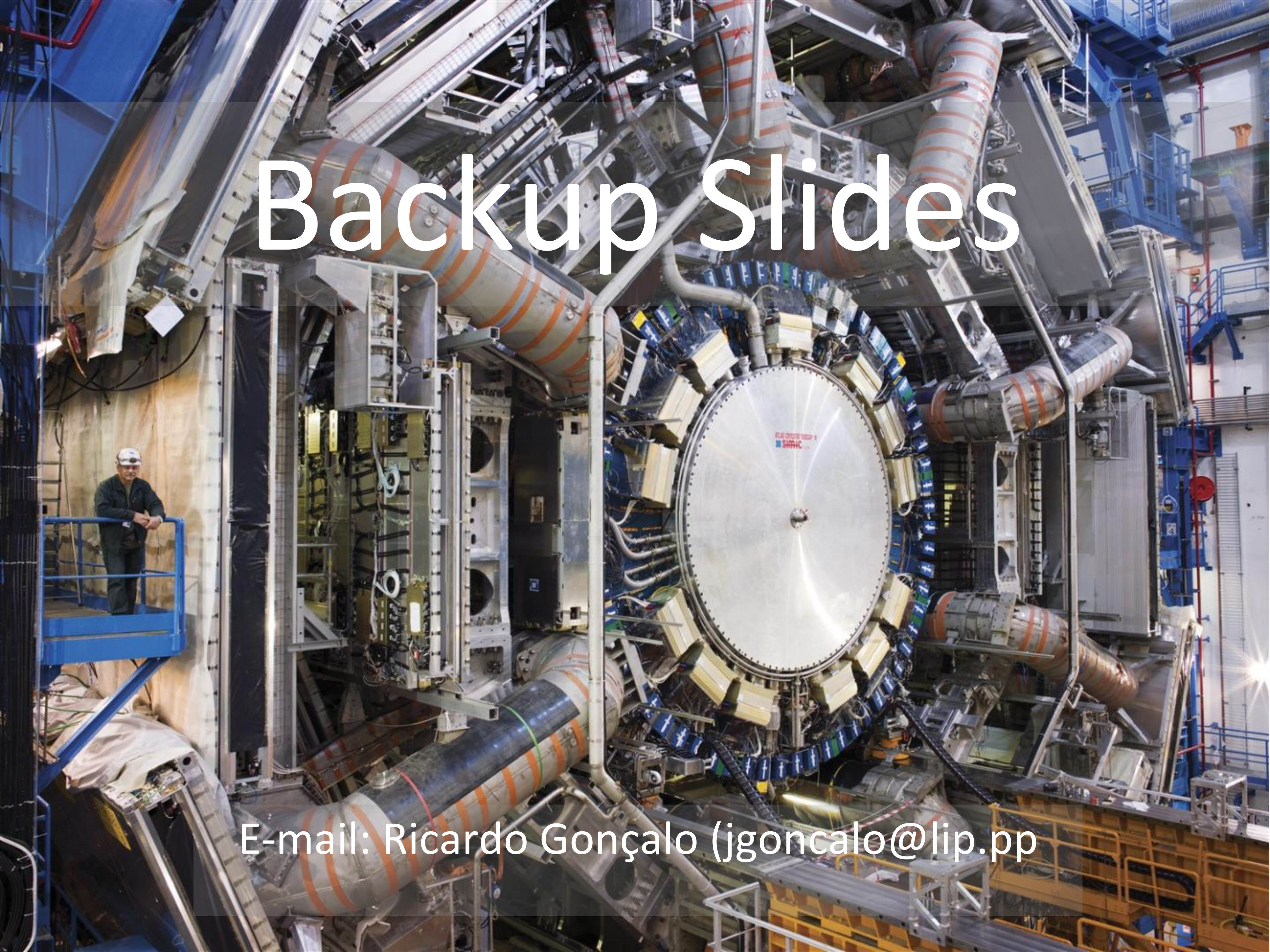


Summary and Outlook

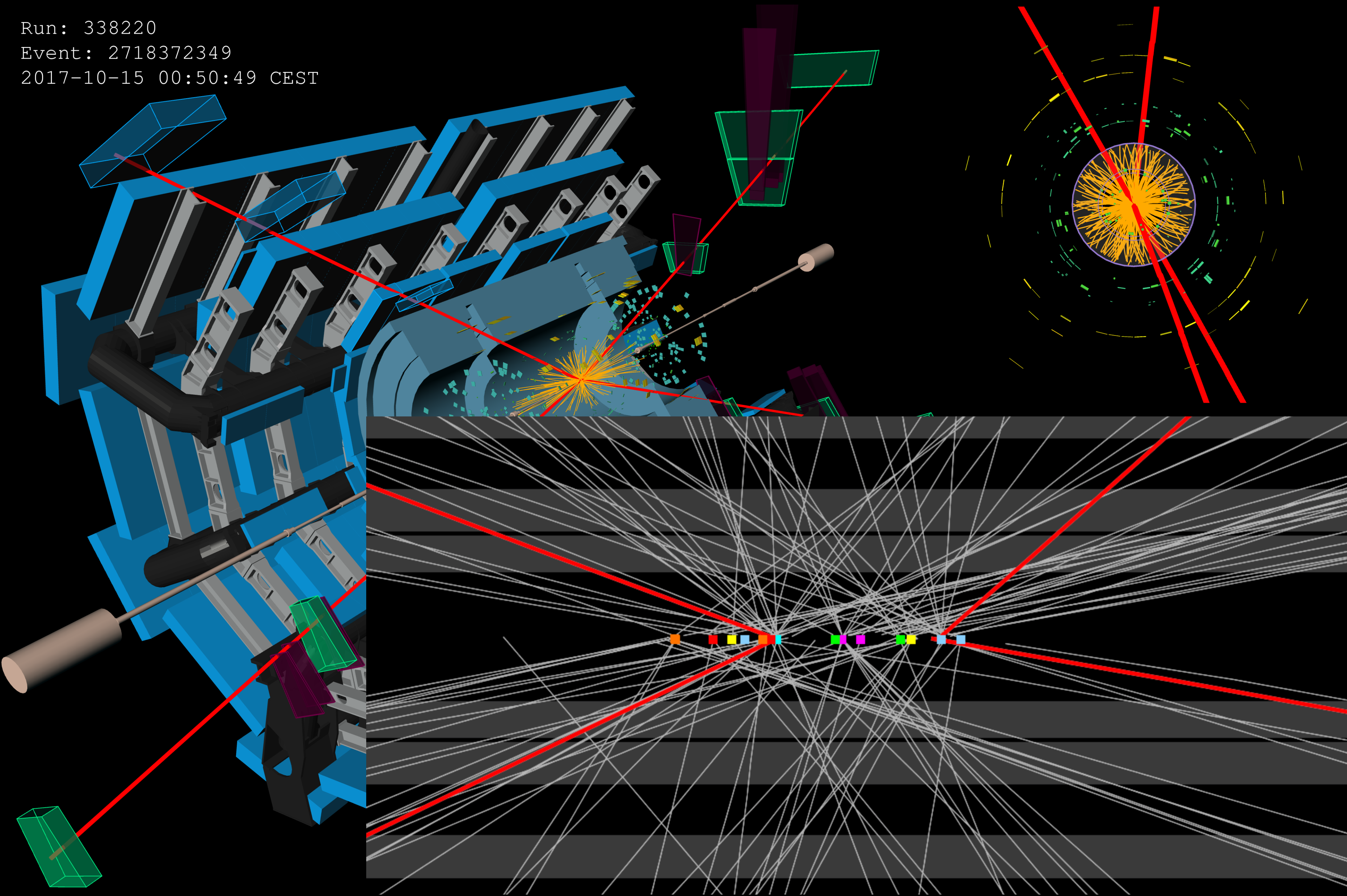
- A lot of activity was started on upgrades for HL-LHC since the last LIP Jornadas
- Interesting times!
  - First HL-LHC run will be on 2029 – 7 years to develop, build, install,and commission – Lots of fun ahead!



Backup Slides



E-mail: Ricardo Gonçalo (jgoncalo@lip.pp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