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Read-out electronics for fast photon detection with COMPASS RICH-1

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Abstract

A new read-out electronics system has been developed for the fast photon detection of the central region of the COMPASS RICH-1. The project is based on multi-anode photomultipliers read out by the high-sensitivity MAD4 preamplifier-discriminator and the dead-time free F1 TDC chip characterised by high time resolution. The system has been designed taking into account the high photon flux in the central region of the detector and the high rate requirement of the COMPASS experiment. The system is described in detail together

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with the measured performances. The new electronics system has been installed and used for the 2006 data taking; it entirely fulfils the expected performances.

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Keywords: Front-end electronics; TDC; COMPASS; RICH; Multi-anode photomultiplier; Particle identification

1. Introduction

The COMPASS experiment [1,2] at the CERN SPS is dedicated to hadron physics with a broad research programme, including the study of the nucleon spin structure using muons as a probe and a variety of issues in charm spectroscopy using hadron beams. The main challenge arises from the need for high luminosity and thus high event rates. All features of the experimental setup are described in Ref. [3].

In the COMPASS spectrometer, hadron identification is obtained with RICH-1 [4], a large size Ring Imaging Cherenkov counter in operation at COMPASS since 2001. During the years 2001–2004, photon detection with RICH-1 has been performed by Multi-Wire Proportional Chambers (MWPC) equipped with CsI photo-cathodes [5], the use of which requires to operate the MWPCs at a rather low gain (below 5×10^4). The first stage of the electronics read-out system was based on a modified version of the front-end Gassiplex-chip [6], amplifying and shaping the signal with a rather long integration time (0.5–1 μs) to compensate for the reduced gain. Since also the baseline restoration time of the Gassiplex output takes about 3.5 μs, a large dead-time is generated. This limited the RICH-1 performance in the COMPASS environment, where uncorrelated background at high rate is present due to a large fraction of muons in the beam-halo. To overcome this limitation and to deal with even higher event rates foreseen for the COMPASS data taking from 2006 onwards, an upgrade of the RICH-1 detector has been proposed and was implemented during the SPS shut-down period between Autumn 2004 and Spring 2006, and was successfully operated during the 2006 and 2007 COMPASS data taking periods.

The RICH-1 upgrade is twofold. In the peripheral region, which amounts to 75% of the active surface, the photon detectors are unchanged since the level of uncorrelated background is not very large. The read-out, however, is now based on a new system [7] with the APV-chip [8] with negligible dead-time and improved time resolution.

The central photon detection area (25% of the active surface) is highly populated by uncorrelated background images with rates up to 1 MHz per channel. Thus a very good resolution of the measured Cherenkov angle is needed to push the limit for hadron identification towards momenta as high as possible. This region is therefore instrumented with a new and fast photon detection system based on Multi-Anode PhotoMultiplier Tubes (MAPMTs) [9], which are coupled with individual telescopes of fused silica lenses to enlarge the effective detection area. The MAPMTs, intrinsically fast and with sub-ns time resolution, are coupled to a read-out system based on highly sensitive amplifier-discriminators and high resolution Time to Digital Converters (TDCs). This read-out system fully exploits the capabilities of the new photon detection system.

The present article describes the electronics read-out system of the MAPMT-based photon detectors. Section 2 gives an overall description of the system, Section 3 reports the main features of the MAPMTs, Section 4 covers in detail the analogue front-end part of the system, while the digital part is presented in Section 5 and the relevant infrastructure and power supplies in Section 6. A summary of the system performance is given in Sections 7 and 8, where the results from laboratory tests and from the COMPASS data-taking in the year 2006 are discussed. Section 9 is dedicated to conclusions.

2. General system description

The read-out system for the MAPMTs is based on the MAD4 preamplifier-discriminator and the high resolution dead-time free F1 TDC, see Fig. 1. All read-out electronics are mounted in a very compact setup as close as possible to the photomultipliers. This setup takes into account the limited space in front of the RICH-1 detector due to the presence of a tracking station mounted directly in front. The read-out system is free from cable connections to minimise the electrical noise, and to obtain a very robust setup.

The lens telescope system as coupled to each MAPMT is shown in Fig. 2 The MAPMTs are mounted in soft iron boxes, which act as magnetic shield against the 200 G

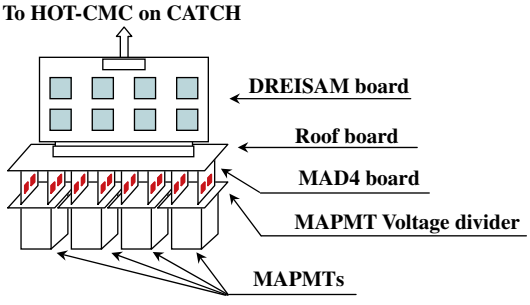

Fig. 1. Schematic overview of the read-out system, a basic unit.

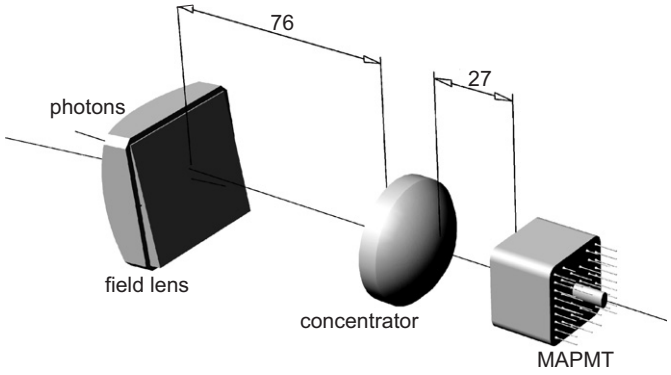

Fig. 2. Scheme of the two-lenses telescope system (distances in mm).

residual magnetic field of the open H-shaped spectrometer magnet placed a few metres upstream of the RICH-1 detector. The iron boxes also house the voltage divider boards, which distribute the appropriate voltage to the MAPMT electrodes and transfer the anode signals to the front-end stage.

The MAD4 boards populated with the MAD4 chips are plugged directly in two connectors on the voltage divider board. The differential output signals of eight MAD4 discriminator boards are fed via the intermediate Roof board to the digital read-out board, the Digital RICH ElectronIc SAMpling (DREISAM) board. The Roof board acts also as mechanical fixation of the read-out electronic boards, and it distributes the Low Voltage (LV) power and the threshold settings to the MAD4 chips.

The digital data from the DREISAM boards are transferred via optical links to the read-out boards: The HOT-CMC mounted on the CATCH boards located in a VME crate at a few metres distance from the detector. From there the data are transferred via S-LINKS [10] to the read-out farm of the COMPASS experiment. The HOT-CMC board has been developed for this project, while the CATCH board is standard in the COMPASS data acquisition system [3].

3. The multi-anode photomultipliers

The MAPMT type R7600-03-M16 by Hamamatsu,[4] with 16 anode channels, bi-alkali photo-cathode and UV extended glass window, has been chosen to detect single photons at high rates, with fast response and in a wide photon wavelength range; for the most relevant parameters see Table 1.

The voltage divider circuit for the power distribution to the MAPMT electrodes has to ensure good efficiency of single photo-electron detection also at high rates. The standard configuration proposed by Hamamatsu for these MAPMTs [11] has been tested in laboratory and test beam studies. No MAPMT gain reduction is observed up to single photo-electron rates larger than 5 MHz per anode [9]. The single photo-electron efficiency, when coupling the MAPMT to the MAD4 amplifier-discriminator (see Section 4) is larger than 95% [9]. This voltage divider configuration has been chosen (Fig. 3).

Table 1
Parameters characterising the MAPMTs used for the COMPASS RICH-1 upgrade

Parameter	Standard value
Photo-cathode surface	$18.1 \times 18.1\,mm^2$ (minimum)
Multiplicative chain	12 dynodes
Gain	3.5×10^6 (typical)
	$(*) > 1 \times 10^6$ at 800 V
Anode DC per channel	0.8 nA (typical)
	$(*) < 2$ nA
Total DC	12 nA (typical),
	60 nA (maximum)
Anode signal rise time	0.83 ns (typical)
Signal transit time	10.9 ns (typical)
Uniformity between anodes	1:2.5 (typical)
	(*) 1:3 (maximum)
QE at 420 nm	>20%
QE at 250 nm	(*) >5%

The standard values are from Ref. [11]; some parameters are required for our application (*).

We use custom, compact voltage divider circuits, which also provide the connection between the MAPMT anodes and the read-out chain. They have been realised as small size PCBs housing surface mounted resistors and capacitors, as well as connectors to the MAPMT pins, on one side, and to the front-end boards on the other side. The main advantage of this compact design is the very short path from the MAPMT anode to the amplification stage: No cables are required. As the voltage divider boards are mounted directly on the MAPMT back side, the layout of the internal copper layers of these multi-layer PCBs is such to prevent almost completely the direct propagation of light through the fibreglass. The PCBs are also varnished in black.

Fig. 4 presents the response of the MAPMT to single photo-electrons: A typical amplitude spectrum is shown. Various spectrum components are clearly distinguishable: At very small amplitudes, the tail of the pedestal signal distribution is visible, followed by two signal peaks. The signal peak at larger amplitudes corresponds to the single photo-electrons that have been multiplied by the whole 12-dynode chain of the MAPMT; the peak at smaller amplitude is due to photo-electrons that have escaped one of the multiplication stages. The typical mean amplitude value of the two peaks at 900 V is 8×10^5 electrons and

[4] *Hamamatsu Photonics K.K.*, http://www.hamamatsu.com.

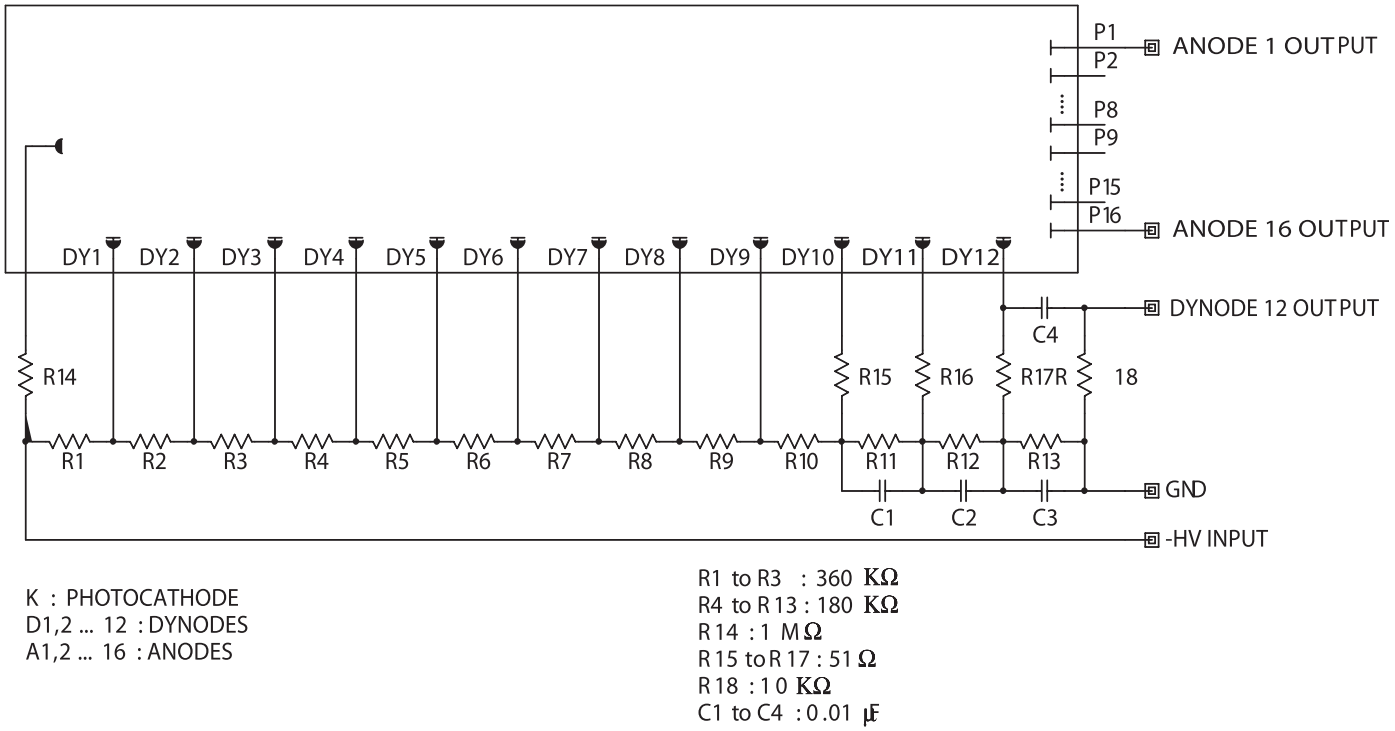

Fig. 3. Scheme of the MAPMT voltage divider.

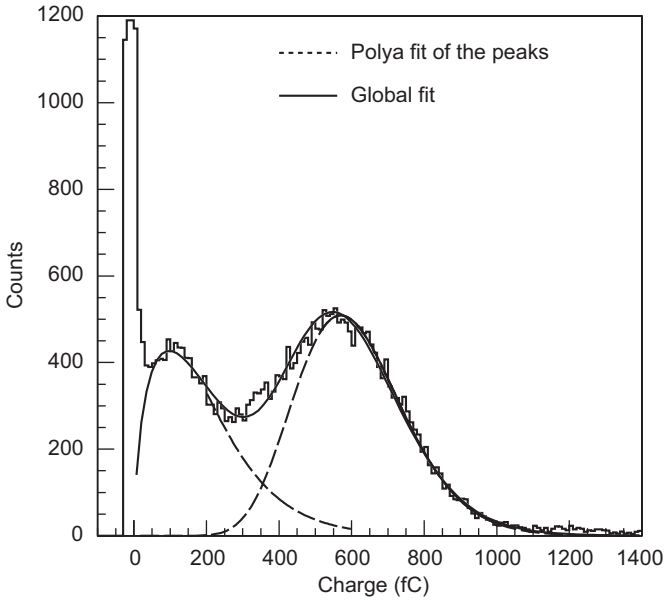

Fig. 4. Typical amplitude spectrum obtained with a MAPMT R7600-03-M16 by Hamammatsu at 900 V illuminating the photo-cathode in single photo-electron mode. The noise pedestal is visible, as well as two signal peaks, the lowest one corresponding to photo-electrons skipping a multiplication stage. The dashed curves are individual fits of the two peaks with Polya functions; the solid curve is a global fit with a sum of two Polya functions.

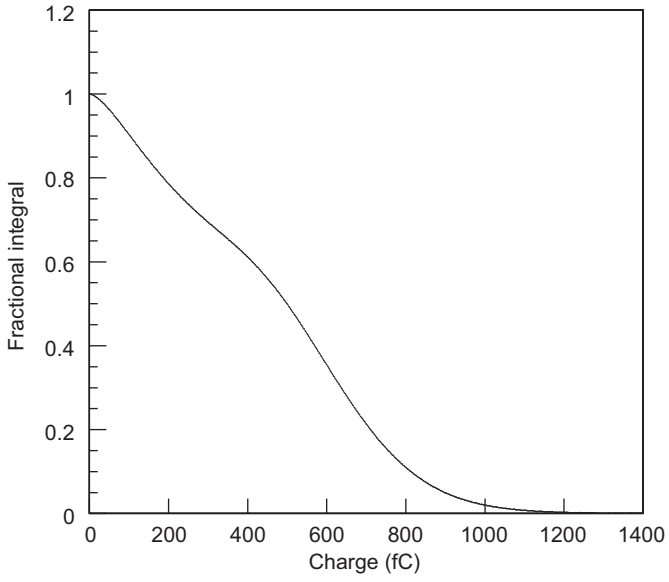

Fig. 5. Normalised integral of the function obtained with the global fit of the amplitude spectrum of Fig. 4 versus the starting point of the integration range.

4×10^6 electrons, respectively. For each MAPMT, the voltage is adjusted to obtain mean values as similar as possible to the typical values indicated above. The applied voltages take into account the spread in gain of the 16 channels of a MAPMT; the measured spread in gain is always below a factor of three. The population of the first peak is always an important fraction of the total population. For our application, the detection of the photo-electron signal of both peaks is equally important. Extremely good efficiency is obtained using the MAD4 amplifier-discriminator, which allows to recover for the spread in gain among the MAPMT channels (Section 4)

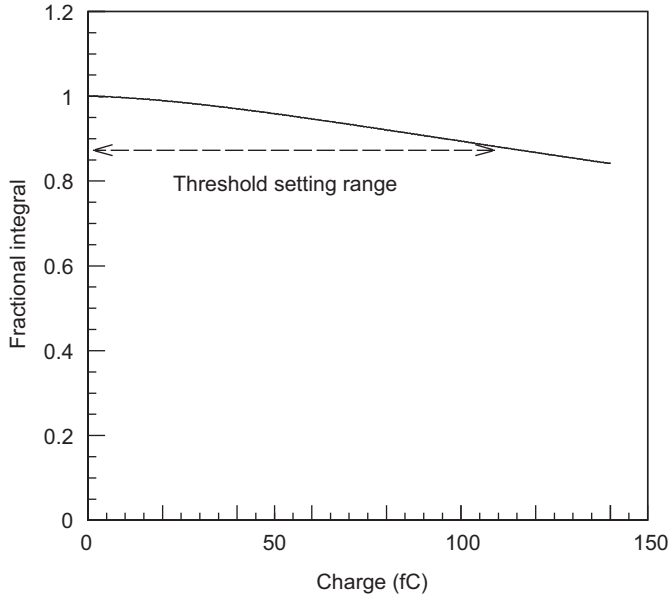

Fig. 6. Zoom of the integral spectrum of Fig. 5; the region of the front-end threshold range is indicated.

and for the different gain of the signals forming the two peaks of the amplitude spectra, without affecting the photo-electron detection efficiency. This is demonstrated in Figs. 5 and 6. Fig. 5 is the normalised integral of the global fit shown in Fig. 4 versus the lower limit of the integration range. In Fig. 6, a zoom of the first portion of the integral spectrum is given and the range of the threshold adjustment is also shown. The typical threshold setting is about 40 fC. This value assures the rejection of the pedestal as well as of the cross-talk signals (Section 7.1.2).

4. Analogue front-end electronics

4.1. The MAD4 board

The main task of the front-end board is to amplify the signals from the MAPMT, to discriminate them and send the differential LVDS signals to the digital board. The MAD4 chip (Fig. 7) is a full custom ASIC in 0.8 μm Bi-CMOS technology developed by the I.N.F.N - Sezione di Padova for the muon drift tubes of the CMS barrel [12]. An integrated circuit includes four channels. Each channel features a charge preamplifier with fixed gain (3.35 mV/fC), a simple shaper with baseline restorer, a comparator, a programmable one-shot to shape the digital output and a LVDS driver. A resistive voltage divider is implemented on the MAD4 board itself (Fig. 8) in order to attenuate by a factor of 2.4 the MAPMT output signal before the preamplification stage, thus avoiding a preamplifier saturation for very large signals. At the preamplifier output, the signal shape is formed by a shaper: A low gain integrator with a small time constant has the non-inverting input pin connected to the preamplifier, while the inverting pin allows to put this stage inside the feedback loop of a low offset Operational Transconductance Amplifier (OTA), thus implementing a baseline restorer. The quiescent level of the baseline is set externally to a fixed voltage VREF common to the four OTAs. The output of this stage is then directly connected to the non-inverting input of a fully differential discriminator. The discriminator is provided with an external threshold common to all the four channels. A logical shaper, the one-shot, follows the comparator stage, allowing a width adjustment of the standard differential LVDS output from 20 to 200 ns. In our application, the width is externally fixed to 40 ns by pin W_CTRL, common to the four channels, see Figs. 7 and 9.

4.2. Roof board

This board has the function of providing services to the MAD4 boards: Power, threshold setting and input/output data transfer from and to the digital board. Each Roof board is directly connected to eight MAD4 boards and a digital board. A voltage regulator provides the 5 V supply to the MAD4 chips. The power consumption per channel is <75 mW. Fig. 10 shows the part of the scheme of the Roof board related to Digital to Analogue Converter (DAC) settings.

Two 8-channel DACs[5] receive 12 bit data words from the DREISAM board: The four most significant bits determine the address of the DAC register, which is loaded with the last eight bits of the data word to set the threshold. The DAC dynamic range depends on Vref_H and Vref_L: $\text{Range} = 2 \cdot (\text{Vref\_H} - \text{Vref\_L}) = 420\,\text{mV}$, see Fig. 11. The VREF reference voltage is fed to the VREF pin of the MAD4, see Figs. 7 and 9, to set the quiescent level of the baseline. The resolution we get from the selected reference voltages is 0.5 fC/digit.

4.3. Front-end characterisation

Several exercises have been performed to determine the design of the input partition optimised in terms of signal attenuation, granularity of the threshold setting, and minimum noise and cross-talk level, see also Section 7. A resistive voltage divider with an attenuation factor of 2.4 has been chosen for the final layout. Before selecting the resistive voltage divider scheme, various layouts with capacitive dividers have been widely tested, but finally excluded due to a slightly higher cross-talk level observed at high rates.

Fig. 12 shows typical threshold curves with three different DAC resolutions. In the second plot, corresponding to the final design (resolution = 0.50 fC/digit), there is a wide range of values for threshold setting outside the noise and cross-talk region with negligible photo-electron losses, as expected (Section 3, Figs. 5 and 6).

The analogue front-end electronics exhibits a small noise in the range of 5–7 fC (Fig. 13), to be compared to the

[5]DAC-8841 by *Analogue Devices*, http://www.analogue.com.

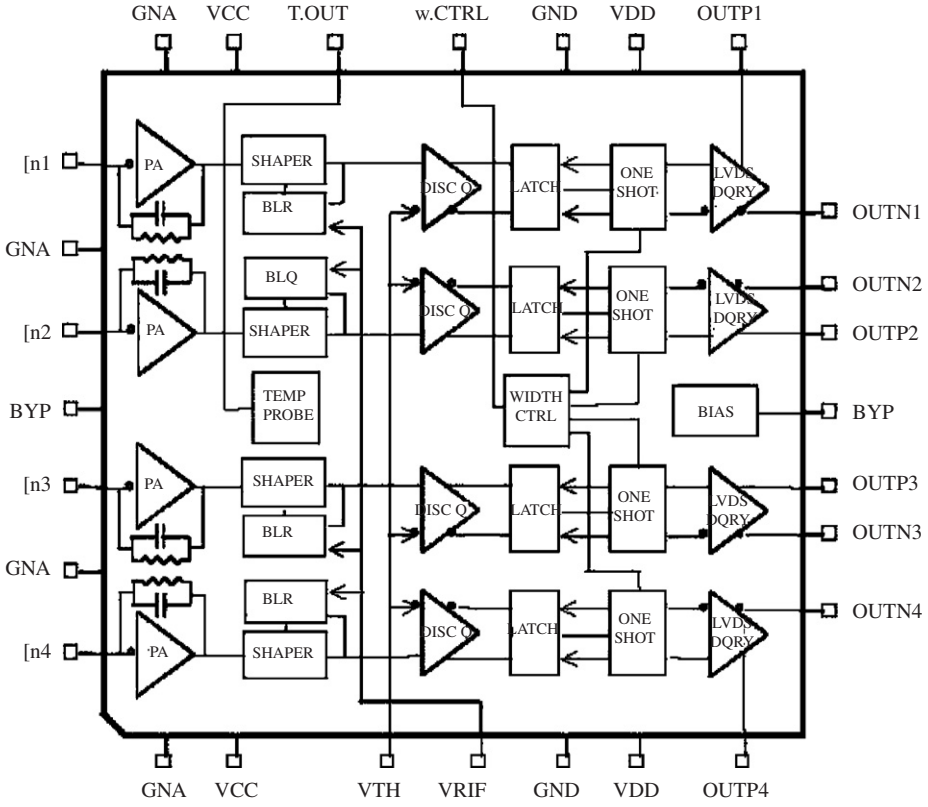

Fig. 7. Block diagram of the MAD4 chip [12].

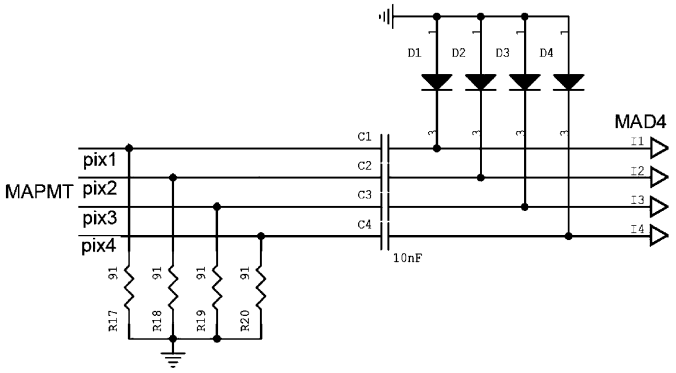

Fig. 8. Scheme of the MAD4 board: The voltage divider.

typical single photo-electron signals of 500 fC, and is capable to sustain an event rate up to 1 MHz per channel, see Fig. 14.

4.4. Production and quality control

In total 144 Roof boards and 1152 (144×8) MAD4 boards are needed to fully equip the area of the new MAPMT-based photon detector of RICH-1. A special board has been designed and produced to pulse independently all the 64 channels of a front-end unit comprising a Roof board and eight MAD4 boards. The coupling of the unit elements is preserved after performing the calibration procedure described in the following.

Each front-end unit has been tested connected to a DREISAM board and using the COMPASS DAQ system [3]. Input signals have been generated from an external pulser and distributed through the charge injecting board to all the 64 channels. Threshold curves for a fixed input charge have been obtained for each channel and the threshold uniformity has been checked. Then a calibration procedure has been applied in order to measure the resolution of each DAC channel. For this purpose, three input pulses of different amplitudes are injected, and the threshold values that cut 90% of the corresponding input signals are determined. Applying a linear fit to these three points, see Fig. 15(a), a resolution value in fC/digit is obtained for each DAC channel, hence for each MAD4 chip input. In Fig. 15(b), the obtained over-all resolution values distribution is shown.

5. Digital electronics

The central part of the digital electronics of the RICH-1 read-out system is the DREISAM front-end board (Fig. 16). It is equipped with eight F1 TDC chips [14] and reads out four MAPMTs. In total, there are 144 DREISAM boards for the read-out of the entire central part of the RICH-1 detector. The data are digitised on the DREISAM boards and transferred via optical links to HOT-fibre CATCH Mezzanine Card (HOT-CMC) boards

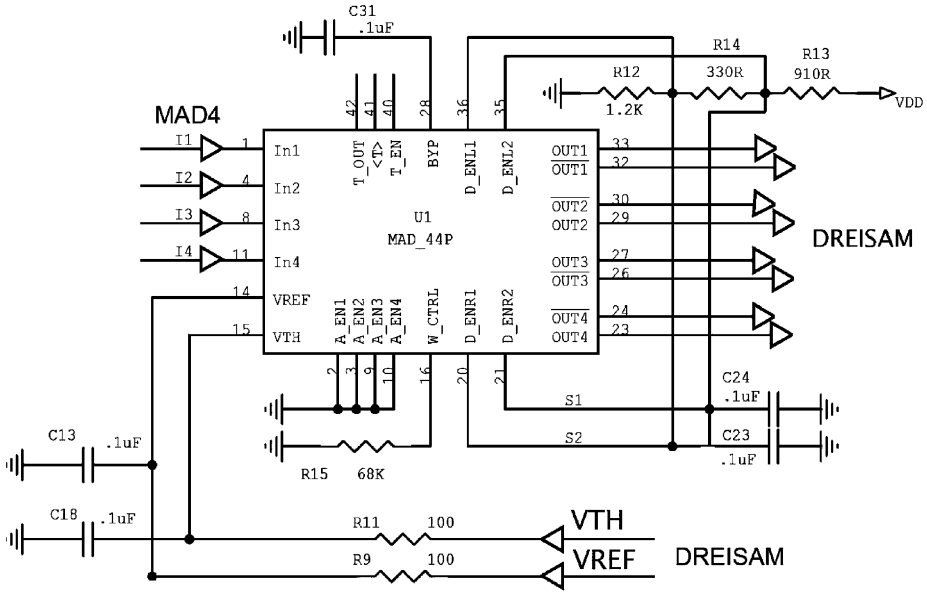

Fig. 9. Scheme of the MAD4 board: The MAD4 chip.

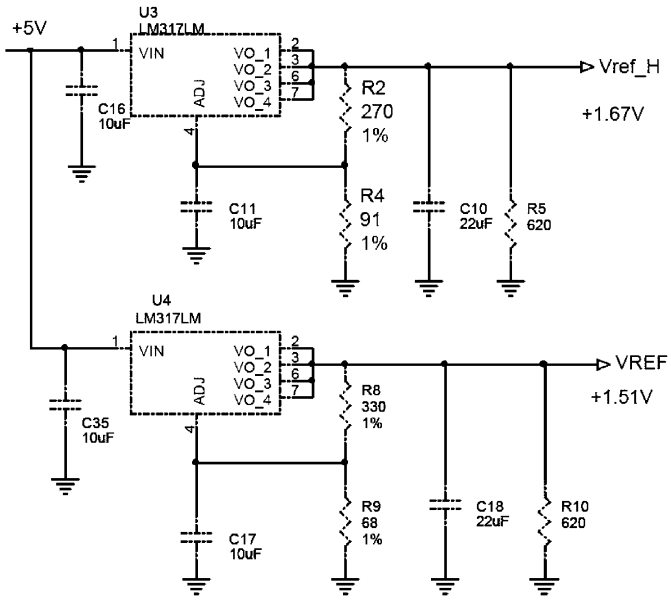

Fig. 10. Scheme of the Roof board: DACs settings.

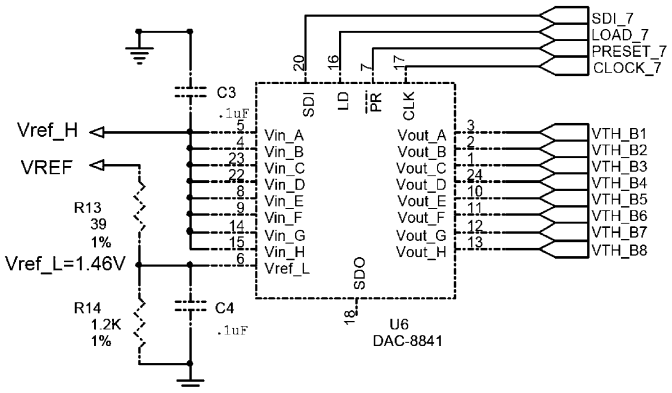

Fig. 11. DACs settings; the scheme of one of the two DACs is shown.

(Fig. 17). Each HOT-CMC receives inputs from four optical links. The HOT-CMC is a mezzanine board, which is plugged into the common read-out driver of the COMPASS experiment: The COMPASS Accumulate, Transfer and Control Hardware (CATCH) [3,14]. On the CATCH, data from four HOT-CMC boards are merged and sent out via S-LINK [10] modules to read-out PCs of the COMPASS data acquisition system [3].

5.1. The F1 chip

The F1 TDC is used for the time measurement of the signals from the RICH-1 MAPMTs. It is a high-resolution dead-time free TDC chip, already used for the read-out of many detectors in the COMPASS experiment. The F1 TDC chip can be operated in different resolution modes, depending on the requirements of the detectors. In Table 2, a list of the available measurement modes of the F1 TDC is given. For the read-out of the RICH-1 detector, the normal resolution mode with eight channels per F1 chip and 100–120 ps digitisation bin width has been chosen. This decision is based on a simulation of the data input and expected trigger rates in the RICH-1 detector estimated from RICH-1 data before the upgrade. In the mode selected, the F1 chip can operate at input data rates of up to 10 MHz per channel and trigger rates of up to 100 kHz. In the COMPASS experiment, all TDCs of various detectors are synchronised by a common 38.88 MHz clock. This clock is distributed by the Trigger Control System (TCS) [3] of the COMPASS experiment. The internal time measuring unit of the F1 TDC is continuously adjusted to this external clock by a Phase Locked Loop (PLL).

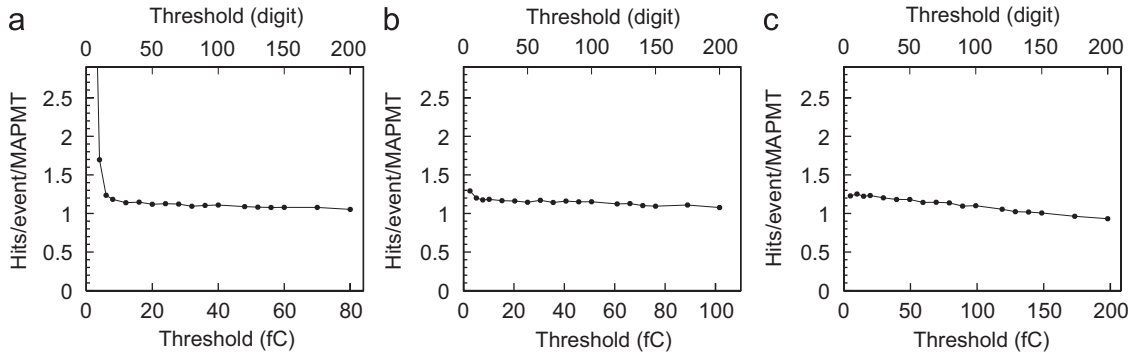

Fig. 12. Threshold curves for three different DAC resolutions: (a) 0.40 fC/digit; (b) 0.50 fC/digit; (c) 0.99 fC/digit; signals are generated by single photo-electrons.

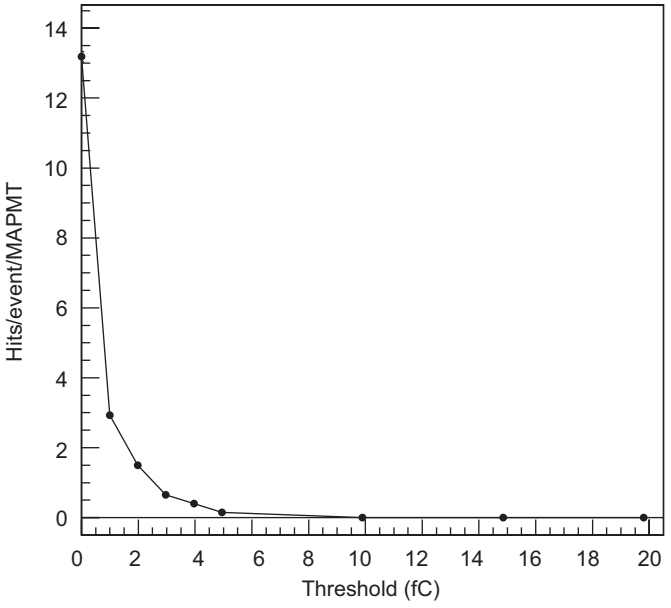

Fig. 13. Noise rates coupling the FE electronics to MAPMT at 900 V, with time gate of 100 ns.

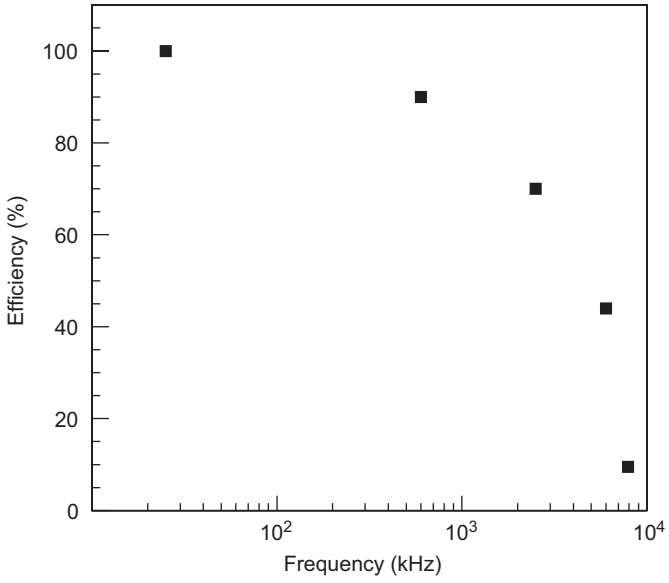

Fig. 14. Measured MAD4 efficiency versus single photo-electron rate.

The relation between the internal measuring time unit and the external clock cycle is defined by two programmable clock division factors, a reference clock divider and a high-speed clock divider. For the RICH-1 read-out, these factors are set to 4 and 25, respectively, which gives a time unit of 108.3 ps for the measurement [15].

5.2. The DREISAM read-out board

The DREISAM board hosts eight F1 TDC chips for the read-out of the RICH-1 detector (Fig. 16). It accepts as input 64 differential LVDS signals, which are transmitted from the MAD4 chips via the Roof boards to the TDCs. The DREISAM board has been designed as a compact 18.0 cm wide and 11.2 cm long 10-layer PCB board. One side of the board is covered by a 0.5 mm thick copper plate at a few millimetres distance from the TDC chips. It carries a water line providing the cooling of the electronics, cf. Section 6.3. The copper plate acts as well as an effective electrical shielding of the TDC chips. Large area ground contact surfaces on both sides of the front-end board guarantee good electrical contact between the front-end board and the copper. Additional ground contacts to the detector are established by connections of the DREISAM board support structure to the RICH-1 frame and by 20 distributed ground pins in the connector to the Roof board.

The data transfer between DREISAM card and CATCH boards is done via two optical links. To avoid any ground loops, there are no cable connections between the RICH-1 electronics and the DAQ system. The optical link is based on two 1 GHz optical transceivers,[6] one on the DREISAM board and one on the HOT-CMC side, respectively. They are connected by a 20 m long multi-mode optical fibre pair.[7] The data from the eight F1 TDC are sent via an 8-bit parallel bus on the DREISAM board to a HOTLINK

[6]JSF-12S2CE2-MJ by *JDS Uniphase*, http://www.jdsu.com.

[7]FPD21-MJ/E2-20 Duplex 62.5/125 (OM1) MTJR/E2000 by *Cabledoc*, http://www.cabledoc.at.

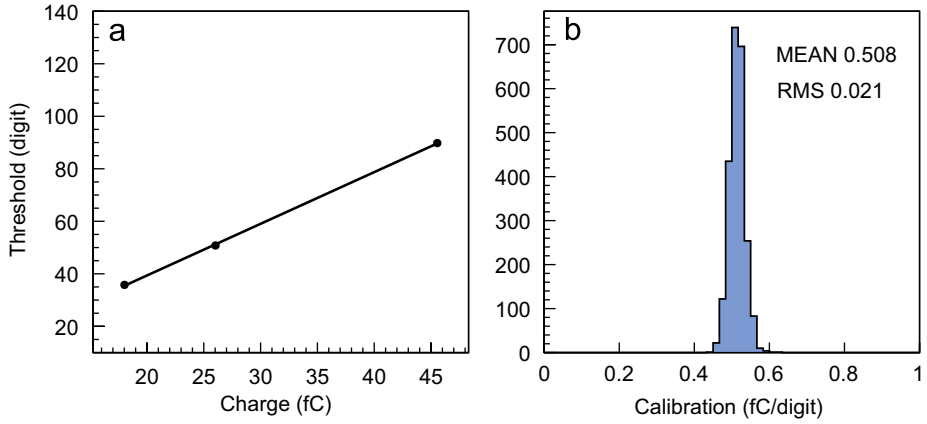

Fig. 15. (a) Calibration of a DAC channel. (b) Distribution of the resolution measured over the whole front-end electronics production.

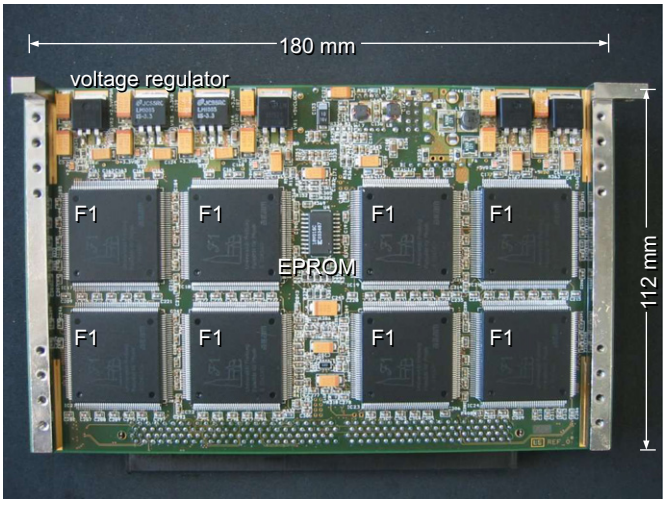

Fig. 16. Front side of the DREISAM board: The eight F1 TDCs can be seen in the lower part of the board. On both sides of the board aluminium bars for mechanical fixation are visible.

encoder chip.[8] In this chip, the 38.88 MHz clocked parallel data from the F1 chip are serialised into a 388.8 MBit/s serial data stream by the HOTLINK protocol. The HOTLINK serial data stream is a DC balanced signal with two additional control bits per byte. It is converted into an optical signal in the transmitter part of the optical transceiver and sent out via the optical fibre to the HOT-CMC.

The encoded signals from the HOT-CMC to the DREISAM board are transferred via a single optical line: These signals are the 38.88 MHz COMPASS synchronous clock, the trigger signals that trigger a read-out of all front-end boards in the experiment, the Begin Of Spill (BOS) signal, which resets all front-end electronics at the beginning of a SPS cycle, and the configuration data. These data define the digitisation bin width for the TDC and the threshold setting for the analogue MAD4 chips. For this purpose, a real-time protocol was developed, which encodes the different signals in a single 38.88 MBit/s data stream (Table 3 and Fig. 18). The data protocol is DC balanced, which is a prerequisite for the AC coupled input stage of the optical transceiver. In addition, it is robust against single bit errors, since an isolated bit error in the default clock signal cannot create a false trigger, BOS, setup or reset signal.

The 38.88 MHz clock is recovered from the serial data stream by a clock recovery PLL.[9] It is then distributed as differential LVDS clock signal to the eight F1 chips. The data from the serial data stream are decoded in a FPGA[10] on the DREISAM board. In addition, this FPGA manages the token handling of the F1 TDC read-out. It can also access the output data stream to add error words in case of errors of the optical link, of the clock recovery or of the TDCs. The firmware of the Virtex I chip is stored in an EPROM[11] on the front-end board. A reload of the FPGA firmware is possible by turning off the transceiver of the optical link in the HOT-CMC for more than 1 ms; this is triggered by a special signal transferred from the VME bus via the CATCH board to the HOT-CMC. A hard reset of the front-end FPGA and a successive reload of the FPGA firmware from the EPROM are performed.

The DACs on the Roof board are programmed via the DREISAM board. The threshold data are stored in internal registers in the F1 TDC chips, and are transmitted via a serial line to the DACs, triggered by a dedicated command to the DREISAM board. To keep the noise level low, the clock for the DAC serial line is turned on only in case new thresholds are loaded.

5.3. The HOT-CMC receiver board

The HOT-CMC (Fig. 19) is a 14.9 cm times 7.5 cm mezzanine board, which receives the data from four

[8]CY7B923-400JC by *Cypress*, http://www.cypress.com.

[9]CLC016-AJQ by *National Semiconductor*, http://www.national.com.

[10]XCV50-4TQ144C by *XILINX*, http://www.xilinx.com.

[11]XC18V01SO20C by *XILINX*, http://www.xilinx.com.

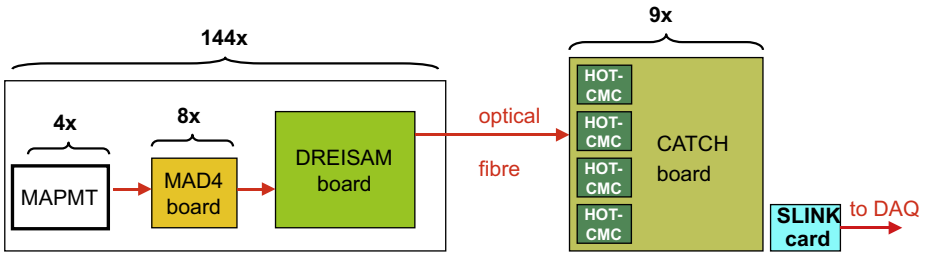

Fig. 17. Scheme of the read-out architecture of the RICH-1 detector.

Table 2
The modes of operation of the F1 TDC chip

Mode of operation	Number of channels/chip	Time unit
Normal resolution mode	8	100–120 ps
High resolution mode	4	50–60 ps
Latch mode	32	5 ns

Table 3
Bit protocol for the data transfer from the HOT-CMC to the DREISAM board

Signal from HOT-CMC to DREISAM	Encoding as bit-pattern
38.88 MHz clock	1010 (continuously sent)
Trigger	100011
BOS	10001011
Setup data bit '1'	1001
Reset signal	10000111

DREISAM boards. It is plugged on the mezzanine connector of the CATCH boards located in a 9U VME crate a few metres away from the RICH-1 detector. On the CATCH boards, the data from the front-ends are checked for errors. Data from 16 front-end boards are then merged and headers with additional information about spill and event numbers are added. Finally, the data from the CATCHes are sent via optical S-LINK links to the PCs of the COMPASS data acquisition [3].

Each HOT-CMC houses four optical transceivers. They receive serial data from the front-end boards by the optical link with a speed of 388.8 MBit/s (Fig. 20). The data are de-serialised by four HOTLINK chips into a 38.88 MHz 8-bit parallel data stream. Errors in the data are detected by the HOTLINK chips by checking the two additional control bits in the data stream (8/10 bit decoding). In case of HOTLINK errors, a LED on the front panel of the HOT-CMC lights up. The data from the front-end boards are buffered in four FIFOs[12] on the HOT-CMC. They are finally transferred to the CATCH by a 40.0 MHz clocked 32-bit bus.

The HOT-CMC receives the trigger, BOS, setup and reset signals from the CATCH board. It encodes these signals with the protocol described in Section 5.2 in a CPLD.[13] The encoded data are transmitted with the 38.88 MHz COMPASS TCS clock. To keep the jitter of the output signal of the CPLD as low as possible, it is synchronised by a high-speed external flip–flop[14] to the COMPASS clock. The optical transceiver uses this signal to generate an optical output and sends it to the DREISAM boards.

5.4. Characterisation

The performance of the DREISAM board was studied in a laboratory setup. For this purpose, LVDS signals were generated in a 1:64 NIM-LVDS converter. An adaptor board transfers the data to the input of the DREISAM board. The maximum trigger and input data rates as well as the time jitter of the TDC measurement have been tested. The DREISAM board has been tested at trigger rates up to 100 kHz. The maximum data input rate on each of the 64 input channels can be 10 MHz. A time jitter of less than 35 ps RMS for every individual channel versus a reference TDC was measured [17].

5.5. Quality control and production

Every DREISAM board was tested in a detailed quality test procedure. For this purpose, a specialised test-software has been developed [16]. Main test items checked in the test procedure are: Functionality, cross-talk between neighbouring channels and time jitter of every channel, and a long-term stability test sampling two million events over 1 h. The correct termination impedance of the LVDS input lines has been verified with a special board designed for this purpose.

6. Infrastructure

6.1. LV supply

The LV power supply for the read-out electronics is provided by six Wiener Power Supply Systems[15] each housing five power supply modules. Due to the power

[12]CY7C4225V-15ASC, *Cypress*, http://www.cypress.com.

[13]XCR3064XL-7VQ44C by *XILINX*, http://www.xilinx.com.

[14]MC100EP131FA by *National Semiconductor*, http://www.national.com.

[15]Modular Floating Power Supply System PL6021, F8, from *WieNeR Plein & Baus GmbH*, http://www.wiener-d.com.

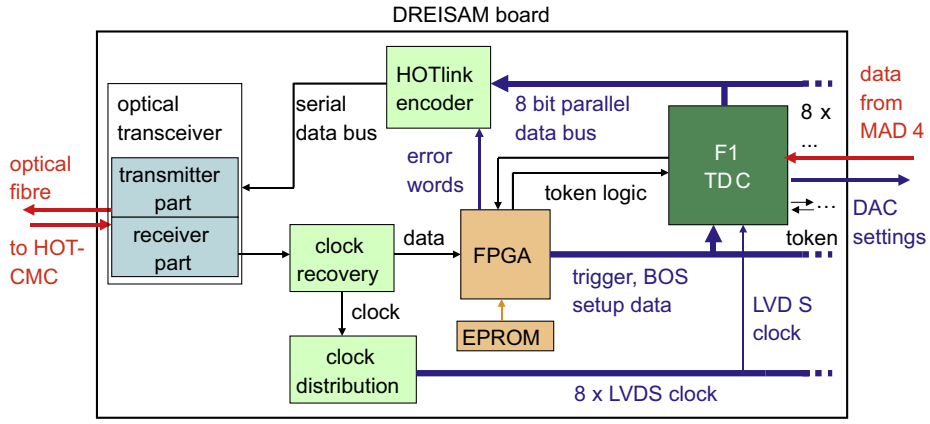

Fig. 18. Block diagram of the DREISAM board.

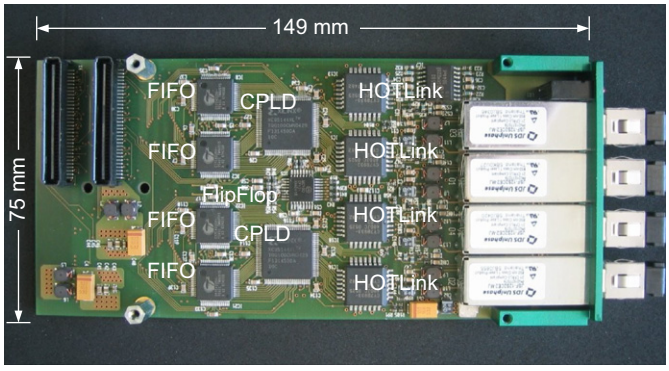

Fig. 19. HOT-CMC mezzanine board. On the right side four optical transceivers can be seen. Next to them the four HOTLINK chips are placed. The mezzanine connector to the CATCH is located on the left side. Next to it the FIFOs are located.

consumption (at maximum hit-rates and running temperature) of the individual MAD4 and DREISAM boards, respectively (Sections 4 and 5) the total power consumption adds up to 85 A and 320 A, respectively. In order to have sufficient safety margin, especially at the switch-on, the power supply for the total detector is distributed via six systems: Two for the analogue part and four units for the digital part. The measured values of power consumption per read-out channel are listed for all parts of the read-out system in Table 4. During data taking, the power supply units are remote controlled by the COMPASS detector control system [3] via CAN (Controller Area Network) bus.

6.2. Mechanical support

The mechanical structure for the components of the read-out system supports them and guarantees good electrical contact between the different boards. It also supports the cooling plates of the electronics cooling system (Section 6.3). Two major challenges have been considered in designing the mechanical support:

- The dense environment formed by the photon detectors, the read-out electronics boards and the cooling plates.
- The request to make local interventions on the read-out elements or on the MAPMTs possible dismounting only limited portions of the setup.

The resulting mechanical arrangement is illustrated in Fig. 21.

6.3. Cooling

The cooling system controls the temperature of the read-out systems of both the MAPMT and the CsI MWPCs. It has been designed to avoid too high temperature of the electronics components and to prevent the formation of temperature gradients inside the RICH-1 vessel. The power consumption for the different components of the MAPMT read-out is given in Table 4. The total power consumption of the MWPC read-out system is about 1500 W.

The cooling system is based on the under-pressure circulation of temperature controlled water in thin copper pipes (1 mm internal diameter) brazed onto copper plates. The cooling plates are in thermal contact either with the mechanical supports of the read-out board (low power consumption components) or with the boards themselves (high consumption components, DREISAM boards) via an elastic thermo-conducting interface material.[16]

The photon detectors are grouped in two sets, a top and a bottom set. The cooling of the two sets is provided by two identical systems (Fig. 22). Each system is formed by a main water container placed at a height lower than that of all the other system components, a set of parallel water lines and a collection vessel. The main water container houses a pump to allow the water flow back from the collection vessel and a heat exchanger to remove the heat brought by the return water. The temperature of the water in the main vessel is kept constant controlling the flow of the chilled water flowing through the heat exchanger. The temperature of the water sent to the cooling lines is fixed at 20 °C, so to avoid the formation of dew on the cooling

[16]Gap-pad ultra soft by *The Bergquist Company*, http://www.bergquistcompany.com.

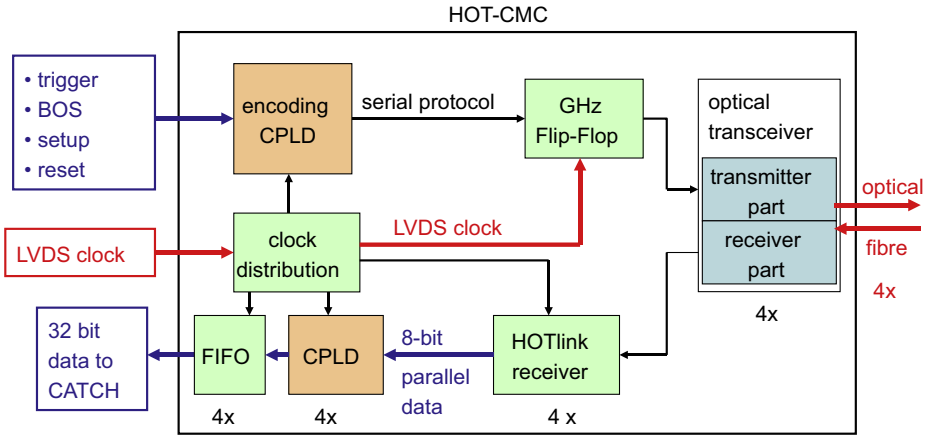

Fig. 20. HOT CMC Block diagram.

Table 4
Power consumption (PCS) of the various elements of the read-out system per read-out channel

Read-out element (total no. of pieces)	Voltage (V) on power supply/board	Current (mA) per channel	PCS (mW) per channel
MAPMT (576)	900	21×10^{-3}	19
MAD4 board (1152)	8/8	8	63
Roof board (144)	8/8	2	16
DREISAM board (144)	9/8	34	309
	6/5.5	6	38
Total			444

The value for the MAPMT includes the voltage divider dissipation.

plates. The water of the cooling line returns to the collection vessel. A pump sucking air from the top of this vessel creates an under-pressure of about −40 kPa. This pump is switched on and off according to the water level in the return vessel. Constantly keeping the under-pressure condition, it ensures that, in case of leakages from a cooling line, the water is sucked back to the main water container and does not fall on the electronics components. A collection pipe let the water flow back from the collector vessel to the main water container. The cooling lines are arranged in a two-stage cascade of manifolds, as illustrated in Fig. 22.

There are three different types of cooling plates: Flat plates for MWPC front-end boards—one per board, U-shape plates for 12 MAPMT voltage divider boards and 24 MAD4 boards—one per a raw of 12 MAPMTs, and flat panels for DREISAM boards—one per board. Temperature sensors placed on some of the DREISAM board cooling plates provide a cooling failure alarm in case of temperature increase.

7. Laboratory tests

7.1. Characterisation of a basic unit

Several tests of a sub-unit consisting of one MAPMT, two MAD4 boards, one Roof board and a DREISAM board have been performed in order to verify that it fulfils the expected performances.

7.1.1. Time resolution

The time resolution of the read-out system has been measured with the test setup shown in Fig. 23. From the time difference of the signals of two MAD4 boards (MAD4-2 and MAD4-3 in Fig. 23) plugged on the same DREISAM board, we get a measurement of the time jitter due to the electronics only, without the contribution of the MAPMT. In Fig. 24, the time spectrum obtained is shown. The time resolution of the read-out electronics system is $110\,\text{ps}/\sqrt{2} \approx 75\,\text{ps}$.

To evaluate the overall time resolution of the photon detector, the MAPMT was included in the read-out chain. A laser head consisting of a laser diode[17] and collimating optic generates optical pulses of a width of $\lesssim 45$ ps. These pulses are sent through an optical filter[18] and 300 μm pinhole onto the MAPMT photo-cathode. The distribution of the MAPMT signal times in response to single photons relative to the trigger time gives the total jitter of the complete read-out system: MAPMT, MAD4 board, Roof board, DREISAM board and the optical fibre, which distributes the clock signal to the TDC. The time spectrum is shown in Fig. 25. The central peak has a width of $\sigma = 320$ ps. In addition, there is a tail of later signals related to photons impinging on the photo-cathode close to the border between two neighboured channels [17].

7.1.2. Cross-talk

The cross-talk between neighbouring channels has been determined by illuminating an isolated MAPMT pixel by a laser diode[19] through a small pin hole of about 300 μm diameter, and measuring the number of hits in the other channels. The results of the measurements are shown in

[17]PiLas EIG1000D by *Advanced Laser Diode Systems GmbH*.
[18]The laser signal density is attenuated by two orders of magnitude using a neutral grey filter in order to have single photons.
[19]PiLas EIG1000D by *Advanced Laser Diode Systems GmbH*.

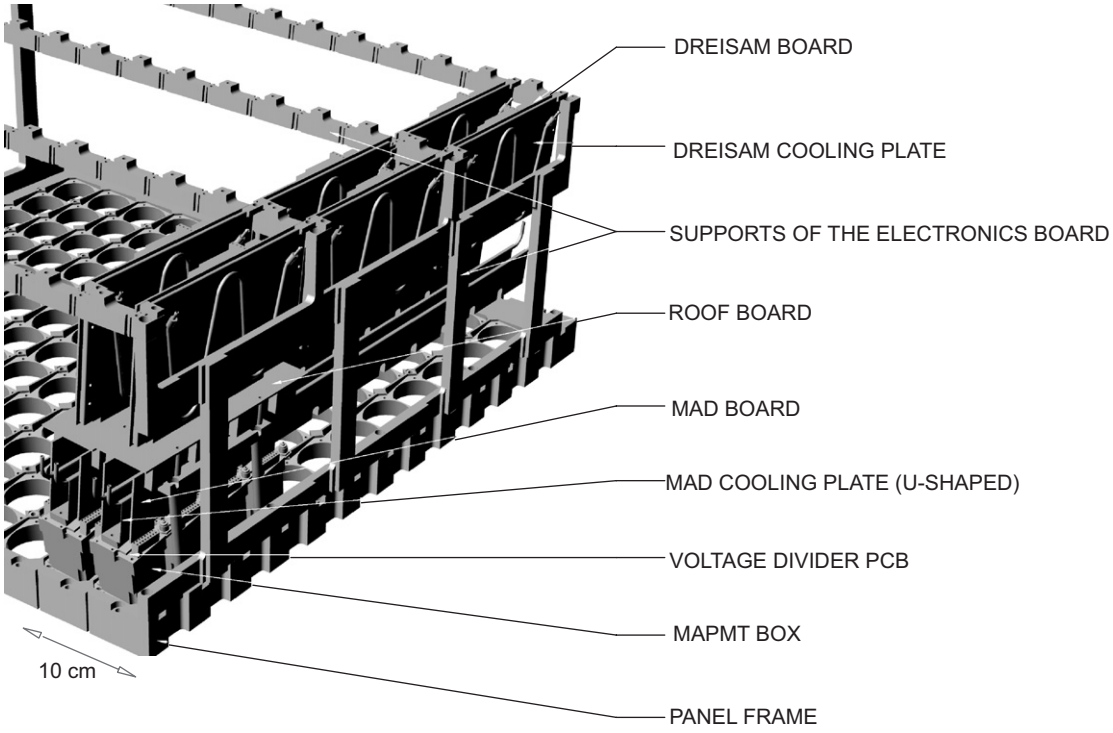

Fig. 21. Design of the mechanical support for one quadrant of the setup.

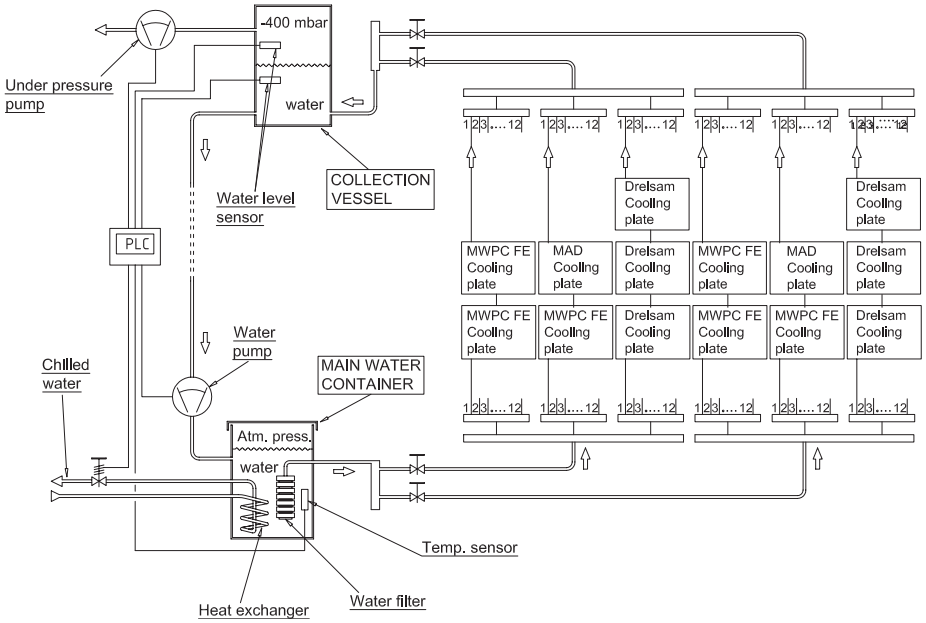

Fig. 22. Scheme of the COMPASS RICH-1 water cooling system.

Fig. 26. The measured cross-talk level for thresholds above 10 fC is well below 10^{-3} for all channels and therefore negligible.

7.1.3. Test of the assembled system

The assembly of the complete first photon detector quadrant (144 MAPMTs), apart from lenses, in laboratory in March 2006 allowed us to verify the effective project quality, concerning all the aspects: Mechanical compatibility, high voltage and low voltage system, noise characterisation, correct mapping of the whole chain, read-out performances. Fig. 27 shows two different moments during the assembly: On the left side, the lens holders, the MAPMT holder frame and the MAPMT iron

boxes are visible; on the right side, the whole quadrant is completely assembled (except lenses). The functionality of all 2304 channels was verified: All the thresholds could be set via the optical links and a low noise level was measured for each channel, consistent with the basic unit test results. The MAPMT photo-cathodes were then illuminated with a LED pulsed by a programmable pulse generator at fixed timing relatively to the trigger: All channels give trigger time correlated hits. The mapping of the whole chain, from the MAPMT pixels up to the DREISAM board channels, was checked. Threshold curves were measured in single-photon mode for a few MAPMTs, showing the expected large plateau well separated from noise and cross-talk region (Section 7.1.2).

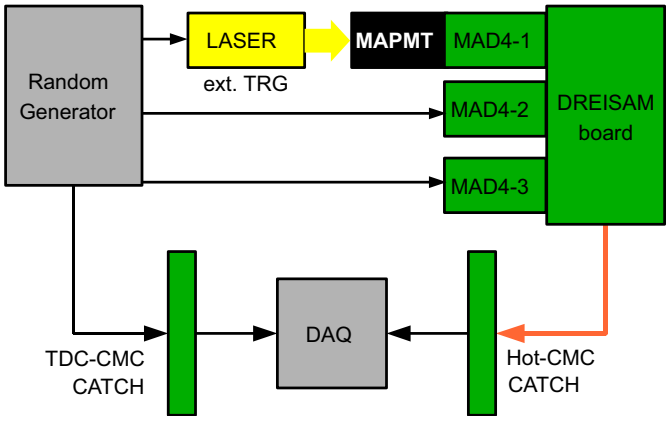

Fig. 23. Setup used for time resolution measurements.

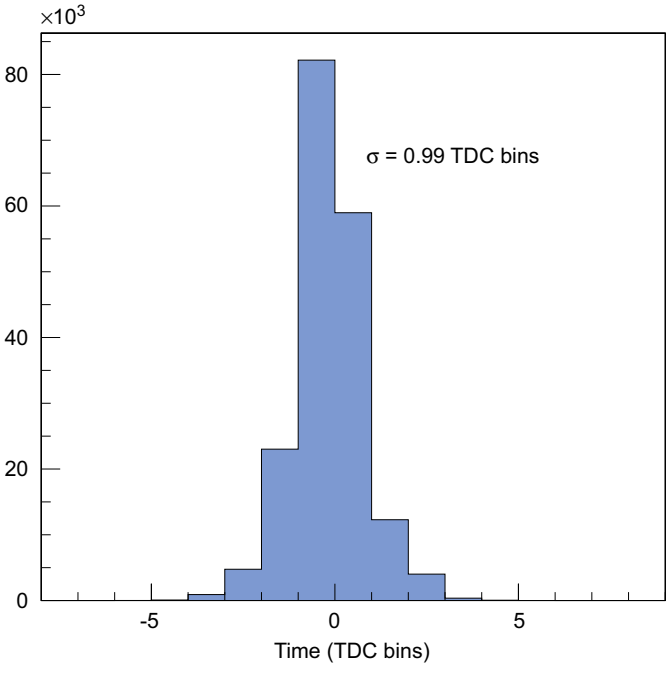

Fig. 24. Time spectrum of the electronic chain (MAD4+ Roof + DREISAM; 1 TDC bin = 108.3 ps).

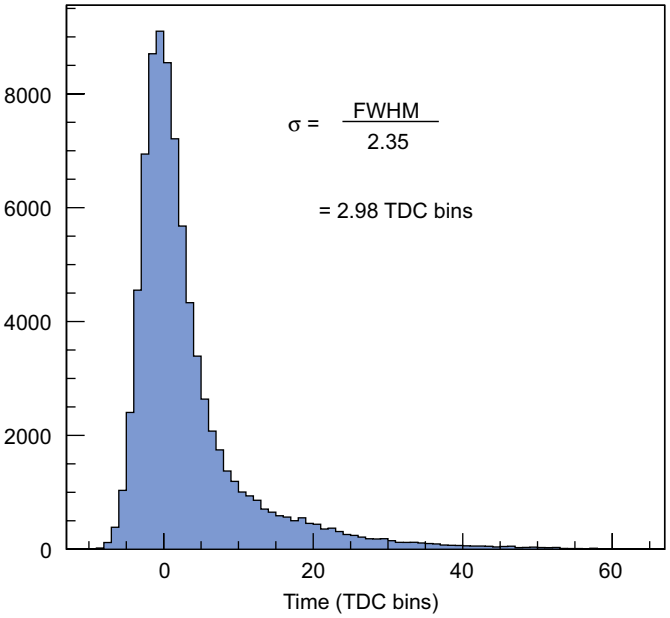

Fig. 25. MAPMT time spectrum (1 TDC bin = 108.3 ps).

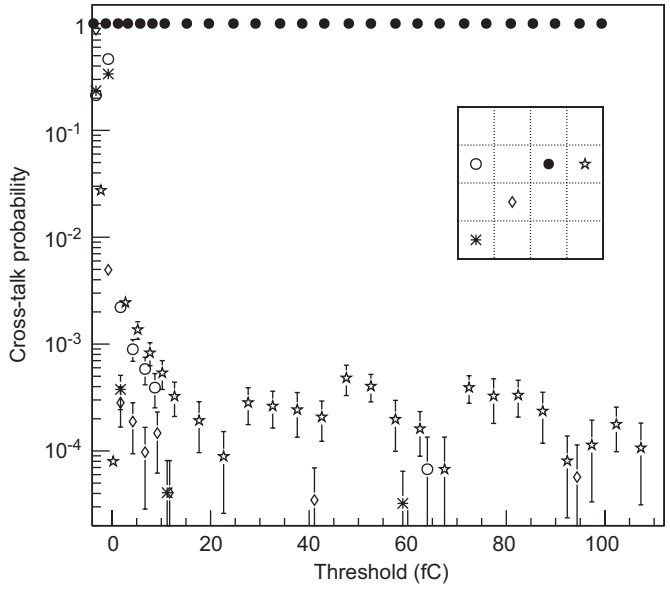

Fig. 26. Cross-talk measurement: Hit rates of the illuminated reference pixel (closed circle) and in different neighbouring channels, each normalised to the reference pixel.

7.2. LED illumination system

Inside the vessel of the RICH-1 detector, two LEDs are mounted in the centre of the front wall below the upper and above the lower photon detector. The light from the two LEDs is reflected by the mirror wall and illuminates the full photon detector. With the LED pulses, the functionality of all channels of the photon detector can be monitored during the detector operation. The LEDs receive their electrical input signals via BNC cables from a

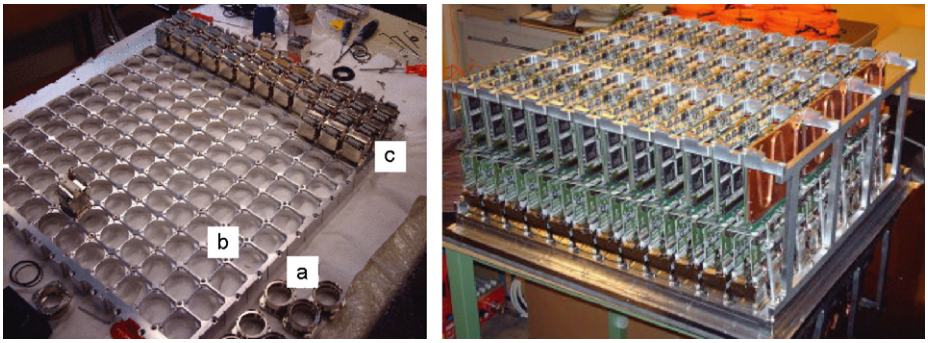

Fig. 27. First quadrant assembly—Left: (a) Lens holders, (b) MAPMT holder frame, (c) MAPMT iron boxes, Right: Completely assembled quadrant of the read-out system with support bars, upper and lower support columns for the front-end boards and the support frame for the digital electronics; three DREISAM water cooling plates are exemplary mounted in the front.

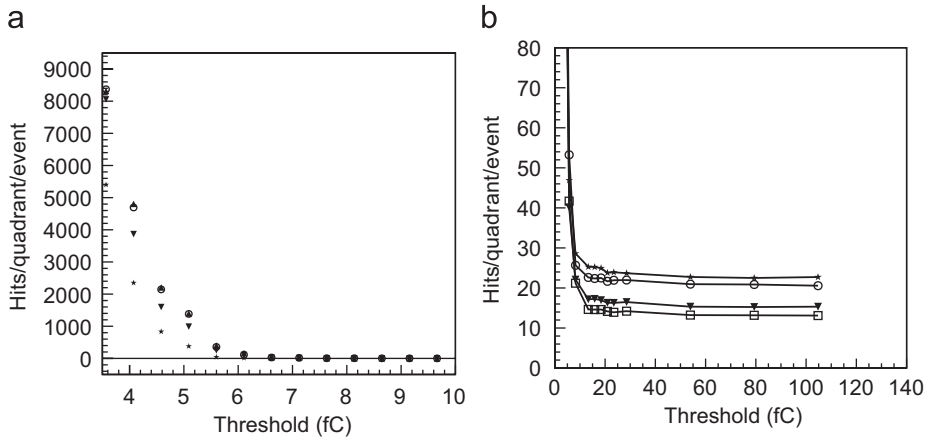

Fig. 28. Threshold curves for the four quadrants. (a) Beam off (b) beam on; the different plateau levels correspond to different particle rates in the different detector quadrants (time window: 100 ns).

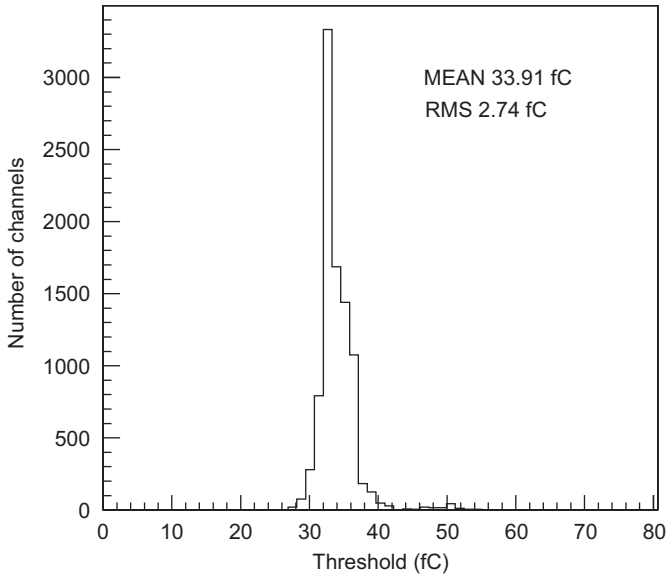

Fig. 29. Distribution of the final threshold setting.

custom-designed pulser module in the RICH read-out VME crate. The programmable pulse generator [18] is a remote controlled module, which generates variable pulses of 0–8 V amplitude and pulse lengths between 10 and 200 ns. For the standard operation of the LED, a pulse length of 10 ns and an amplitude of 4–5 V has been chosen.

8. Performances in the real environment

After more than one year long break due to the shutdown of the CERN SPS, COMPASS data taking was resumed in 2006. In this section, we present the performances of the read-out system of the MAPMT-based photon detectors in the COMPASS environment during the 2006 data taking.

8.1. Noise and cross-talk in real environment

The electronics noise has been measured channel by channel in the real environment with beam off, in order to find the correct threshold over noise value for each MAD4 chip. In Fig. 28(a), the obtained threshold curves for the four quadrants are shown: The noise level is lower than 7 fC, like in the laboratory studies. To evaluate the cross-talk level, another threshold scan has been performed with beam on for threshold values above noise level. The obtained threshold curves are shown in Fig. 28(b). The cross-talk level is negligible above 35 fC. The distribution

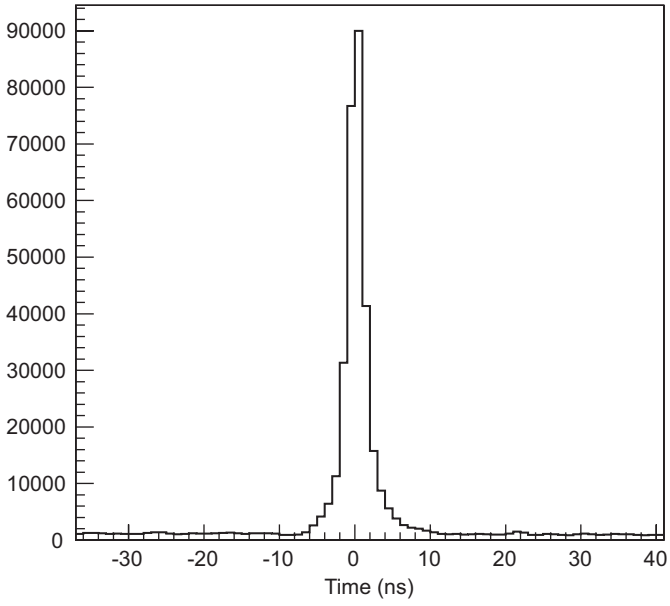

Fig. 30. Physics signal and background—real environment, for details see text.

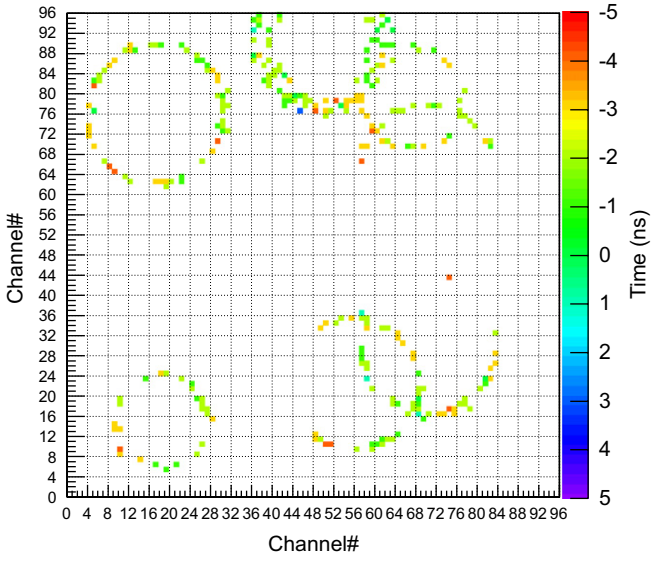

Fig. 31. Online single event display: Hadron-generated Cherenkov rings detected in 2006.

of thresholds set during the 2006 run for each MAD4 chip is finally shown in Fig. 29.

8.2. Time spectra

In Fig. 30, the time spectrum of a whole quadrant of the MAPMT detector part in data taking is displayed. It shows a peak with a sigma of about 1 ns corresponding to the Cherenkov photons created by particles in the triggered physics events. The width of the peak is determined by the different geometrical path lengths of the photons in one Cherenkov ring travelling from the particle track via the mirrors to the photon detection system. The observed width has been confirmed in a Monte Carlo simulation of the detector setup. The time resolution of the photon detection system itself and the read-out electronics has been measured to be significantly smaller, namely 320 ps (Section 7.1.1).

The background below the peak is created by uncorrelated photons mainly from Cherenkov photons of particles of the muon halo traversing the radiator gas. The time window of the TDC is set to ±50 ns around the physics signal peak. Due to the very good time resolution of the photon detection system, an excellent background suppression is possible by applying a suitable offline time cut of a few ns around the signal peak.

8.3. Hadron Cherenkov rings

The upgraded RICH-1 detector, including the new MAPMT detector part, was successfully commissioned at the beginning of the COMPASS 2006 data taking [19]. The RICH MAPMT online event display showing multiple hadron Cherenkov rings detected in a single physics event is shown in Fig. 31. The time window applied is ±5 ns: The time resolution of a few ns within a single Cherenkov ring can be appreciated. While the hardware time window of the TDC has been set to ±50 ns around the trigger time, an offline time cut of ±5 ns is applied to the data. The average number of detected photons per ring is about 56 for saturated rings and the resolution on the Cherenkov angle is about 0.3 mrad [20].

9. Conclusion

We have presented the front-end electronics of the MAPMT-based photon detectors of the central part of the RICH-1 of the COMPASS experiment at CERN. This project is part of the complete upgrade of RICH-1, designed to withstand the high rate foreseen for the COMPASS data taking from 2006 on. The compact design, the good matching between the MAPMT and the MAD4 amplifier-discriminator chip, and the performances of the digital board, based on the F1 chip, allows a high efficient, low noise and very stable front-end chain.

The system has been largely tested in the laboratory and installed in the real environment before the 2006 data taking period. The performances obtained, both in the laboratory and in the experimental conditions, described in detail in the article, entirely fulfil the original design.

Acknowledgements

The authors are grateful to the colleagues of the COMPASS Collaboration for constant support and help. This work was supported in part by the BMBF (Germany) and the European Community-research Infrastructure Activity under the FP6 programme (Hadron Physics, RII3-CT-2004-506078).

References

[1] The COMPASS Collaboration, Proposal, CERN/SPSLC/96-14, SPSC/P297, March 1, 1996, addendum, CERN/SPSLC/96-30, SPSLC/P297, Addendum 1, May 20, 1996.

[2] E.S. Ageev, COMPASS Collaboration, et al., Phys. Lett. B 612 (2005) 154;
V.Yu. Alexakhin, COMPASS Collaboration, et al., Phys. Rev. Lett. 94 (2005) 202002;
E.S. Ageev, COMPASS Collaboration, et al., Eur. Phys. J. C 41 (2005) 469;
E.S. Ageev, COMPASS Collaboration, et al., Phys. Lett. B 633 (2006) 25;
V.Yu. Alexakhin, COMPASS Collaboration, Phys. Lett. B 647 (2007);
E.S. Ageev, COMPASS Collaboration, et al., Nucl. Phys. B 765 (2007) 31;
V.Yu. Alexakhin, COMPASS Collaboration, Phys. Lett. B 647 (2007) 330;
M. Alekseev, COMPASS Collaboration, et al., Eur. Phys. J. C 52 (2007) 255;
M. Alekseev, et al., COMPASS Collaboration, Phys. Lett. B, accepted for publication.

[3] P. Abbon, COMPASS Collaboration, et al., Nucl. Instr. and Meth. A 577 (2007) 455.

[4] E. Albrecht, et al., Nucl. Instr. and Meth. A 502 (2003) 112;
E. Albrecht, et al., Nucl. Instr. and Meth. A 502 (2003) 236;
E. Albrecht, et al., Nucl. Instr. and Meth. A 502 (2003) 266;
E. Albrecht, et al., Nucl. Instr. and Meth. A 518 (2004) 586;
E. Albrecht, et al., Nucl. Instr. and Meth. A 553 (2005) 215.

[5] RD26 Collaboration, Status Reports: CERN/-DRDC 93-36, 94-49, 96-20; The ALICE Collaboration, Technical Design Report of the High Momentum Particle Identification Detector, CERN/LHCC 98-19, ALICE TDR 1, 14 August, 1998; F. Piuz, Nucl. Instr. and Meth. A 502 (2003) 76.

[6] C. Santiard, et al., Gassiplex: a low noise analog signal Processor for readout of gaseous-detectors, Presented at the Sixth Pisa Meeting on Advanced Detector, La Biodola, Isola d'Elba, Italy, May 1994.

[7] P. Abbon, et al., Nucl. Instr. and Meth. A 567 (2006) 104.

[8] M.J. French, et al., Nucl. Instr. and Meth. A 466 (2001) 359.

[9] M. Alekseev, et al., Nucl. Instr. and Meth. A 553 (2005) 53;
P. Abbon, et al., Nucl. Instr. and Meth. A 567 (2006) 114;
P. Abbon, et al., Nucl. Instr. and Meth. A 572 (2007) 419;
P. Abbon, et al., Studies for a Fast RICH, World Scientific, Singapore, 2006, p. 103, ISBN 981-256-798-4.;
P. Abbon, et al., Nucl. Instr. and Meth. A 580 (2007) 906;
P. Abbon, et al., Nucl. Phys. B Proc. Suppl. 172 (2007) 75;
P. Abbon, et al., Czech. J. Phys. 56 (2006) 318;
P. Abbon, et al., Czech. J. Phys. 56 (2006) 327;
P. Abbon, et al., Czech. J. Phys. 56 (2006) 333;
P. Abbon, et al., Nucl. Instr. and Meth. A 581 (2007) 419.

[10] H.C. van der Bij, et al., IEEE Trans. Nucl. Sci. NS-44 (1997) 398.

[11] HAMAMATSU, Multianode Photomultiplier tube assembly H8711, Technical Data.

[12] F. Gonnela, M. Pegoraro, CERN-LHCC-2001-034, p. 204.

[14] H. Fischer, et al., Nucl. Instr. and Meth. A 461 (2001) 507.

[15] TDC-F1 Functional description, ACAM Messelektronik, D-76297 Stutensee, ⟨www.acam.de⟩.

[16] H. Wollny, Diploma Thesis, University of Freiburg, March 2007.

[17] R. Hagemann, Diploma Thesis, University of Freiburg, August 2007.

[18] D. Setter, Diploma Thesis, University of Freiburg, April 2005.

[19] P. Abbon, et al., Nucl. Instr. and Meth. A 580 (2007) 906.

[20] G. Pesaro, Diploma Thesis, University of Trieste, May 2007.