R&D PROJECTS IN COLLABORATION WITH CERN

2000

TECHNICAL ANNEX

Collaboration in the CMS Experiment

22nd September 2000

Sumário do Projecto

Título:

COLABORAÇAO NA EXPERIENCIA CMS

Sumário:

O LIP é membro da experiência Compact Muon Solenoid (CMS) no acelerador Large Hadron Collider (LHC) actualmente em construção no CERN. O objectivo da experiência é o estudo de colisões de protões a muito alta energia. Pretende-se investigar as propriedades fundamentais da matéria e, em particular, estudar a natureza da quebra de simetria na interacção electrofraca e a origem da massa.

A actividade do LIP centra-se no desenvolvimento de hardware e software para o *trigger* de calorimetria e para o sistema de leitura de dados do calorímetro electromagnético. O projecto é desenvolvido em colaboração com o INESC.

O *trigger* de calorimetria da experiência CMS/LHC no CERN é um sistema electrónico e computacional de elevado desempenho que processa em-linha os dados do detector provenientes de cerca de cem mil canais, para seleccionar electrões, fotões, *taus* e eventos com energia perdida, assim como amostras de acontecimentos *jet*. O sistema de *trigger* executa a primeita etapa do processo de selecção na pesquisa de novas reacções físicas, em particular a pesquisa do bosão de Higgs. A escala do problema é várias ordens de grandeza acima dos sistemas actuais, atendendo ao grande número de canais a processar e à elevada taxa de repetição do colisionador LHC (40 MHz). Em resumo, o sistema de *trigger* de calorimetria de CMS é um processador massivamente paralelo, operando em modo *pipeline*. Microelectrónica e ligações ópticas de ponta são usados no projecto. O*trigger* de calorimetria é composto de quatro sistemas principais: o Gerador de Primitivas de Trigger (TPG), o Trigger Regional, o Trigger Global e o Sistema de Controlo.

O Calorímetro Electromagnético (ECAL) é um detector de electrões e fotões composto por oitenta mil cristais PbWO4 de grande pureza. A granularidade extremamente fina e a excelente resolução em energia tornam este instrumento particularmente bem adaptado para a medida de electrões e fotões no LHC. A luz de cintilação dos cristais é convertida por fotodíodos de avalanche (APD), digitalizada e transferida do detector através de ligações ópticas de alta velocidade (1 Gbit/s). O sistema de leitura de dados é responsável pela recolha dos dados em 80000 ligações ópticas, armazenamento em memórias *pipeline*, formatação e verificação da integridade dos dados e transmissão para o sistema DAQ. O sistema é composto por 50 *crates* VME 9U. Cada *crate* aloja 17 módulos Trigger/Readout, 1 módulo de concentração de dados (DCC) e um CPU de controlo.

PROJECT SUMMARY

Project Title:

COLLABORATION IN THE CMS EXPERIMENT

Summary:

LIP is a member of Compact Muon Solenoid (CMS) experiment at the Large Hadron Collider (LHC) presently in preparation at CERN. The experiment aims at the study of very high energy collisions of proton beams. Investigation of the most fundamental properties of matter, in particular the study of the nature of the electroweak symmetry breaking and the origin of mass, is the experiment scope.

The LIP activity is centered on the development of hardware and software for the calorimeter trigger and for the readout system of the electromagnetic calorimeter. The project is carried on in collaboration with INESC.

The calorimeter trigger system of the CMS/LHC experiment at CERN is a high performance electronics and computing system which processes on-line the detector data, about one hundred thousand calorimeter channels, to select electrons, photons, taus and missing energy events, as well as, samples of jet events. The trigger system performs the first selection step in the search for new physics reactions, in particular the search for the Higgs boson. The scale of the problem is several orders of magnitude above the trigger systems developed so far, given the large number of channels to process and the very high repetition rate of the LHC collider (40 MHz). In short, the CMS calorimeter trigger system is a massive parallel processor, working in pipeline mode. State-of-the-art microelectronics and data links are used in the project. The calorimeter trigger is composed of four main systems: the Trigger Primitive Generators (TPG), the Regional Trigger, the Global Trigger and the Readout & Control System.

The Electromagnetic Calorimeter (ECAL) is an electron and photon detector composed by eighty thousand high purity PbWO4 crystals. The extremely fine granularity and the excellent energy resolution makes this instrument very well suited for the measurement of electrons and photons at the LHC. The crystal scintillation light is converted by avalanche photo-diodes (APD), digitized and transferred from the detector through high speed (1 Gbit/s) optical links. The readout system is responsible for collecting data from 80000 detector links, storage in pipeline memories, event formatting, data integrity checking and data transmission to the DAQ system. This system is composed by about 50 VME 9U crates. Each crate houses 17 Readout/Trigger Boards, 1 Data Concentrator Card (DCC) and one controller CPU.

Information on the CMS Calorimeter Trigger project is available at
http://cmsdoc.cern.ch/ftp/afscms/TRIDAS/caltrig/html/CalTrig.html

Information on the ECAL Readout and Trigger at
http://rsl3eth2.cern.ch/CMS-ECAL-Electronics/

PROJECT DESCRIPTION

1. INTRODUCTION

In April 1998 the CMS Resources Review Board formed by representatives of the Financing Agencies approved the CMS Memorandum of Understanding for the construction phase. In this document the Portuguese responsibilities are defined as follows:

- ECAL, Barrel Electronics: Responsibility to provide trigger and upper-level read-out electronics.
- ECAL, Endcaps Electronics: Responsibility to provide trigger and upper-level read-out electronics.
- Trigger/DAQ, Calorimeter Trigger: Responsibility to provide the control and read-out system.

Portugal has well defined construction responsibilities in the CMS Trigger/DAQ and ECAL projects.

The LIP participation in the Tracker project is for the moment restricted to R&D of the tracker alignment system. The continuation of this R&D program in 2001 is the object of a separate proposal.

At the present time, the Portuguese team in CMS puts together members of the LIP, INESC and IST in Lisbon, and of the University of Porto and INEGI at Porto in a total of about 20 people.

During the last five years, the R&D activity of the LIP group on the CMS experiment was supported by the Portugal-CERN Scientific Program. The present proposal addresses the continuation of this work: we request financing support for the final prototyping activities to be carried out during 2001, prior to the start of production foreseen in 2002.

2. THE CMS CALORIMETER TRIGGER AND ECAL READOUT

The calorimeter trigger system of the CMS/LHC experiment at CERN is a high performance electronics and computing system which processes on-line the detector data, about one hundred thousand calorimeter channels, to select electrons, photons, taus and missing energy events, as well as, samples of jet events. The calorimeter trigger is composed of four main systems: the Trigger Primitive Generators (TPG), the Regional Trigger, the Global Trigger and the Readout & Control System.

The Electromagnetic Calorimeter (ECAL) upper level readout system is responsible for collecting data from 80000 detector channels, storage in pipeline memories, event formatting, data integrity checking and data transmission to the DAQ system. The system is composed by about 60 VME 9U crates. Each crate houses 17 Readout/Trigger Boards (ROSE100), 1 Data Concentrator Card (DCC) and one controller CPU.

The Trigger Primitive Generators are physically located in the calorimeters readout boards (ROSE100 modules). The trigger primitives are synchronized and transmitted to the Regional Trigger through high speed links located in the ROSE100's transition boards (Sync and Link Board).

The participation of LIP is concentrated in the following items (see Figure 1):

- Development and construction of the trigger synchronization circuits and the trigger high-speed links (construction of 850 Synchronization and Link Boards).
- Development and construction of the ECAL Data Concentrator Card (construction of 60 DCC 9U VME boards).
- Development and construction of the calorimeter trigger readout and control system, both hardware and software. This system will use a simplified version of the ECAL Data Concentrator Card (Trigger Data Concentrator). Construction of 20 PMC trigger readout boards and 5 TDC boards. Control software running of 20 trigger VME processors and trigger back-end servers.
- Development of software for the ECAL readout prototypes. Control software running on 60 ECAL VME processors.

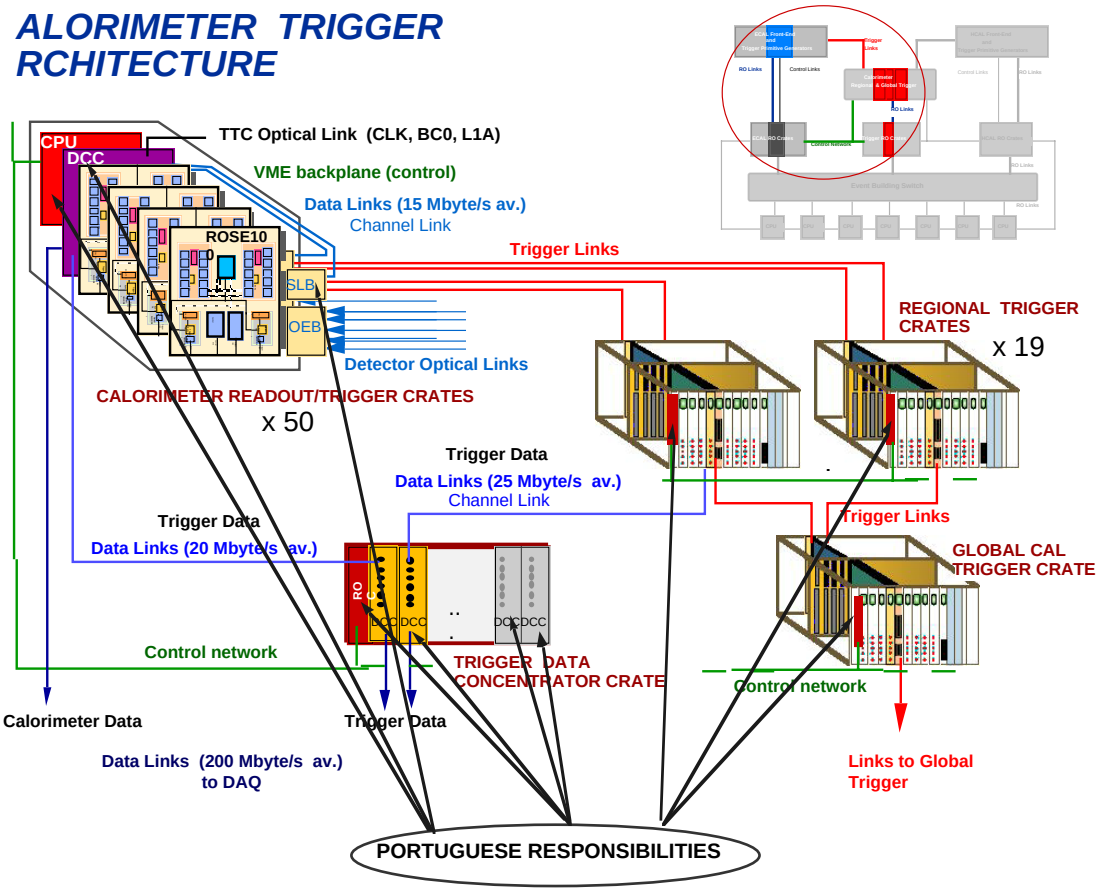

Figure 1

The general planning of the ECAL and Trigger/DAQ projects foresees that the present prototyping phase will continue up to the end 2001 when the final design will be frozen. A pre-production will be made in the year 2002 and full production and installation in the years 2003-2004.

The following institutes participate in the project:

ECAL Readout/Trigger module (ROSE100)	CERN, Palaiseau, ETHZ, Lisbon
Synchronization and Link Board	Lisbon
ECAL DCC and readout software	Lisbon
Regional Trigger	Wisconsin
Global Calorimeter Trigger	Bristol
Trigger Readout and Control	Lisbon

A major milestone of the Trigger Project is the submission to LHCC of the Trigger Technical Design Report on November 2000. A draft version of the Trigger TDR was already submitted to the CMS Collaboration and to the CMS internal referees. LIP takes a very active role in this work, having full responsibility for Chapter 7 (Calorimeter Trigger Readout and Control), Chapter 16 (Trigger Control), Chapter 17 (Synchronization and Latency) and shares responsibility in Chapter 3 (Calorimeter Trigger Introduction) and Chapter 4(Calorimeter Trigger Primitive Generation).

3. PROPOSED R&D PROGRAM

The program proposed for 2001 is driven by the construction responsibilities that the LIP group has assumed within the CMS experiment. The program is divided in the following sub-projects.

In sub-project 1 we plan to develop the final version of the Trigger Synchronization circuit. The basic functionality of the synchronization circuits is established and was confirmed after the tests with two prototype versions. Control quality issues of the Sync are addressed in sub-project 5.

Sub-project 2 aims at the development of the final prototype of the trigger primitives generator and ECAL readout modules (ROSE100). This project will be carried out in collaboration with Palaiseau, CERN and ETHZ. LIP is responsible for building the Sync/Link Board, which includes the Synchronization circuits (sub-project 1), and the Trigger and Data Acquisition data links. A first prototype was built and tested. Next year we intend to build the final prototype, test the trigger links, and test the integration with the DCC prototype (sub-project 3).

Sub-project 3 aims at the conclusion of the design and test of the ECAL Data Concentrator Card prototype. This prototype receives data from the Sync/Link Board (sub-project 2), and will profit from the test environment developed for sub-project 2. The high-level simulation of the DCC will be continued in the framework of sub-project 5.

Sub-project 4 is a software project which aims at the continuation of the development of the trigger control system. This software is used to control the ECAL and Trigger hardware prototypes developed in the framework of sub-project 2.

Sub-project 5 addresses the issues of quality control. The sub-project includes three tasks, namely the reliability of the Sync circuit, the application of boundary scan at system level and the development of high-level models of the system. This effort is mainly conducted by INESC and represents the continuation of the activities developed this year.

Figure 2 shows in diagrammatic form the interrelations between these five sub-projects.

Finally sub-project 6 aims at the development of on-line monitoring software for the ECAL beam tests and sub-project 7 contemplates the computing activities in the framework of the development of the simulation, reconstruction and analysis software of the CMS experiment.

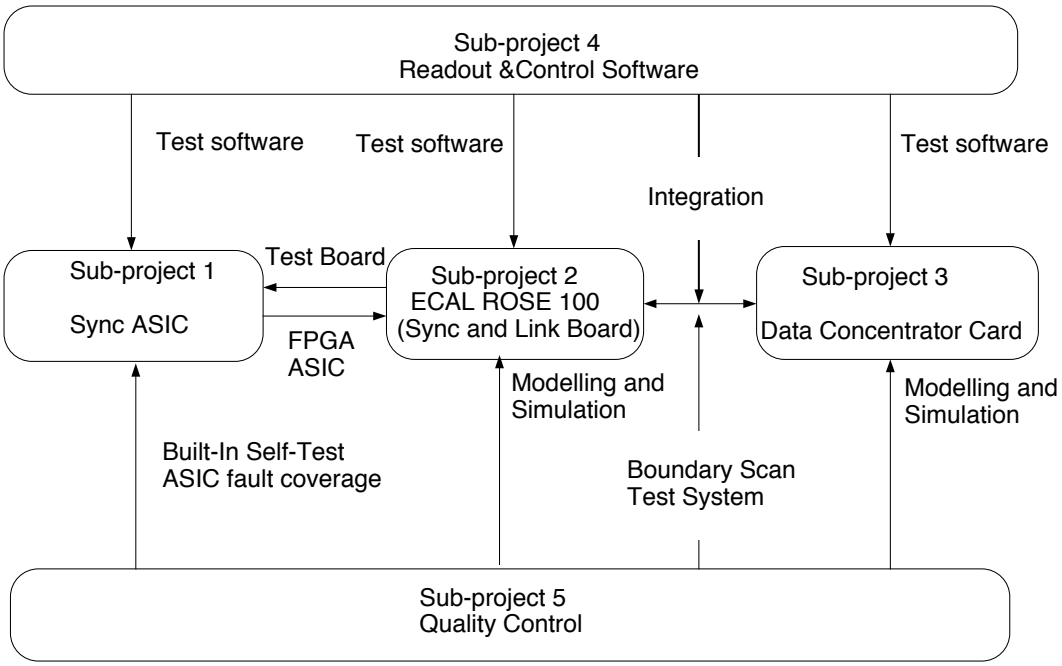

Figure 2- Interrelation between the sub-projects.

Sub-Project 1

THE TRIGGER SYNCHRONIZATION CIRCUIT

Data synchronization is one of the most challenging tasks to be performed by the trigger and data acquisition system of the CMS experiment at LHC. The LIP group developed a method to achieve data synchronization in the context of the CMS synchronous and pipelined trigger system. The method is physically implemented by synchronization circuits associated to each trigger data link.

In 1997 LIP, in collaboration with the Portuguese microelectronics company TECMIC, has developed prototype versions of these circuits (SyncTx and SyncRx) as well as a test setup which demonstrated the performance of the synchronization method.

Based on this experience, in 1998-99 we have redesigned the circuit in order to integrate the two circuits in one (SyncTx/Rx), adding at the same time some test functions. The specification of the new circuit was written and the design of the functional blocks was done at TECMIC.

The design of the Built-In-Self-Test (BIST) of the SyncTx/Rx was done at INESC and implemented in 99-00.

The test of the proto-99 done at LIP during last year showed some instabilities that were traced back to limitations of the technology used.

The next and final phase of this sub-project it is the development of the final prototype. Two main modifications with respect to previous prototype will be introduced, namely the migration to a faster technology and the merge of two Sync Tx/Rx in a single circuit. This last modification is dictated by integration requirements at the system level.

We plan to use a programmable gate array technology, which provides flexibility and avoid the NRE costs characteristic of ASICs development. The unit cost of these devices is now very attractive and within our construction budget.

Quality control issues on the SyncTx/Rx circuit are addressed in sub-project 5.

Sub-Project 2

ECAL READOUT AND TRIGGER MODULE (ROSE100)

1. Project Status

The prototype ECAL readout and trigger modules (ROSE100) developed in previous years consists of a motherboard (VME 9U) and a number of daughter boards that implement the various functions. The list of boards, functions and responsibility is the following:

Mother Board	Interfaces and Control	CERN, ETHZ
Receiver Board	Optical receivers, deserializer	CERN, Palaiseau
Pipeline Board	Data pipelines	CERN
TPG Board	Primitives generator and filters	Palaiseau
Sync/Link Board	Synchronizer, trigger and DAQ links	Lisbon

The SLB prototype built by LIP was successfully tested in a dedicated test system built on purpose (Figure 2). The present SLB prototype includes all the functionality except the trigger links, due to delays in the delivery of the Vitesse components.

The remaining daughter boards indicated above were developed by our collaborators and tested in standalone mode. Due to a problem with the high density connectors used in the Mother Board the integration test that was planned for this year was not concluded. Partial integration tests, namely the test of the Sync/Link Board together with the TPG Board, are planned for this fall.

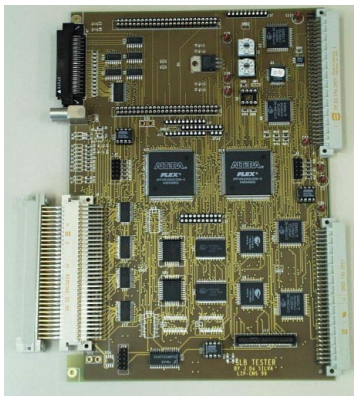

Figure 2. Left) SLB prototype; Right) SLB Tester

2. Proposed Program

The Sync/Link Board is a transition card of the ROSE100 Readout/Trigger Card, connected to the backplane in the rear part of the VME crate. It performs both trigger and ECAL readout functions.

In the trigger path, the Sync/Link Board synchronizes the trigger primitives (synchronizer circuit) and sends serialized data through the trigger link to the Regional Trigger. In this prototype the Sync proto-99 circuit is used (see sub-project 1). The SLB performs readout function as well, in particular it contains the links to the DCC (Channel Link). Interfaces to the TTC system and to the Boundary Scan test protocol are provided.

The design of the trigger link is made in collaboration with the University of Wisconsin, which will use Vitesse receiver chips in their design of the regional trigger. Delays in the delivery of the Vitesse links as well as temporary shortage of manpower at Wisconsin delayed this development. The test of the trigger links are now planned for next year. In parallel LIP started the test of an alternative solution based on the Channel Link from National.

Due to construction budget constraints, the number of different boards in the system should remain as low as possible. Also we know that in large systems interconnections are responsibly for a large fraction of the system failures. However, the use of daughter or transition boards permits to distribute better the design and testing tasks among the institutes involved, and makes the debugging and maintenance easier. At present we are studying the final system architecture. One possibility under consideration is to merge the input Receiver Board and output Sxnc/Link Board in a single transition board.

We foresee a production of sixteen boards. The 16 boards cover 32 trigger towers and represent about 1% of the final system. These boards will be integrated with the ECAL front-end electronics in the framework of the test of large-scale prototypes of the CMS crystal calorimeter.

3. Resources

LIP will use existing development tools for the design and simulation of the Sync/Link Board. The test setup is based on the existing LIP infrastructure.

We request financial support to build the next generation of the Sync/Link Boards prototypes.

One electronic engineer (full time) and a software engineer (half time) will be attached to the sub-project.

Sub-Project 3

PROTOTYPE OF THE DATA CONCENTRATOR CARD

1. Project Status

1.1 Trigger readout

We have built a first prototype of the Local Readout Unit (LRU) in the trigger. The LRU is implemented as a PMC (PCI Mezzanine Card) in the crate processor. Serial links connect the crate LRUs to the Trigger Data Concentrator Cards (TDCC). The TDCC is a simplified version of the ECAL DCC, which is also under our responsibility (see next).

The first prototype was used to evaluate different serial link technologies (IEEE 1394, Firewire and Channel Link, National). The final choice was made (Channel Link from NI).

1.2 ECAL readout

LIP is responsible for developing, prototyping and building the Data Concentrator Cards (DCC). The DCC is a 9U VME module responsible for collecting data from 20 sources, performing event formatting, data integrity checking, and transmission to the central Data Acquisition System. The final system will include 60 DCCs, one per ECAL readout/trigger crate.

Our group has developed the concept of ECAL selective readout for reducing the amount of data to be collected without damaging the physics. Simulation studies were performed in order to estimate data volumes and impact on physics.

A study of selective readout implementations and an architectural design of the data collection were performed. Preliminary system simulations were done in order to estimate buffer sizes and readout latencies.

The design of the DCC is now well advanced and a detailed document of specifications was produced.

2. Proposed Program

The test of the DCC prototype will be one important activity next year. The work is split in two complementary tasks:

- DCC design, production and test
  The detailed engineering design of the DCC prototype will be concluded. We foresee to produce the first DCC prototype in the first trimester of 2001. The DCC prototype will then be test together with SLB boards.
- DCC simulation
  A high-level modeling and simulation of the DCC, and its integration in the ECAL readout system based on object-oriented techniques, will be pursued by the INESC group (see sub-project 5). The simulations are important to determine some of the DCC final design parameters. The input to the DCC hardware simulation are physics events simulated with ORCA , the CMS simulation package (see sub-project 6)

3. Resources

LIP will use existing CAD tools for the design and simulation of the DCC prototype. The test of the DCC will use the 9U VME crate bought these year. We request support for the construction of the DCC prototypes as well as for the acquisition of a VME processor necessary to the test facility.

Two engineers will be attached to the sub-project, one responsible for the high-level model and the other responsible for the electronics design and test. A software engineer (part-time) will provide software support.

Sub-Project 4

TRIGGER READ-OUT AND CONTROL SOFTWARE

1. Project Status

The main objective for 2000 was to deliver a major version of the Calorimeter Trigger Readout and Control System. This release, an almost full functional experimental prototype for the Trigger Readout and Control System, should include:
a. all the functionality, identified so far, for operating an ECAL Front-end Sub-system;
b. all the functionality, identified so far, for operating the ECAL Trigger hardware prototypes, including prototype components for the readout, trigger primitive generation (TPG) and trigger primitive synchronization and transmission (SLB).

While the first part of this objective is still under way, the second was accomplished partially on time.
Hence, looking back to the past year we have planned for:

Sep. 1999 - Dec. 1999: the design, implementation and test of software for all the Front-end Calorimeter Trigger hardware components. This phase was intended to include the delivery of test software for all the Front-end Calorimeter Trigger hardware components, including the calorimeter read-out, the trigger primitive generation and its synchronization and transmission. In fact we have only delivered test software for the readout and the trigger primitive synchronization and transmission. The rest of the software is waiting for the availability of the remaining hardware components to be developed.

Sep. 1999 - Mar. 2000: the design, implementation, integration and test of the control and data transmission software component (DCP) for the Calorimeter Trigger Readout and Control System. The objective of this phase was to assess and solve the problems inherent to the data transfer and the inter-process communications in a distributed environment. Its outcome should be a standalone, single crate, Calorimeter Trigger Readout and Control System. But, as mentioned at that time, this task depended on finding a suitable partner for its execution. Since we haven't find such a partner, it was decided to continue it on our own using 'components off-the-shelf' (COTS). As a result, this task is still under way and is expected to last until the end of this year.

Apr. 2000 - Jun. 2000: the implementation, test, installation and deployment at CERN of a remote controlled Calorimeter Trigger Readout and Control System version including a dual-crate Front-end Sub-system. This phase depended on the previous one and therefore is now scheduled to the end of this year. Instead, during this period, we made a first attempt to integrate the current H4 Test Beam software with our own software.

Jul. 2000: the participation in the Pre-calibration of the first CMS ECAL Super-modules in the H4 beam line. This phase was postponed to July 2001 since the Pre-calibration of the first CMS ECAL Super-modules, itself, was postponed to July 2001.

Jul. 2000 - Dec. 2000: the design, implementation and test of software for the Calorimeter Regional Trigger hardware. This task depended on the availability of the Regional Trigger hardware prototypes. Due to the unavailability of those prototypes it was postponed also.

Dec. 2000: the implementation and test of a standalone Calorimeter Trigger Readout and Control System version including a single (or dual) crate Front-end Sub-system and a single crate Regional Trigger Sub-system. This phase also depended on the previous one and therefore is subject to the same delay.

Concurrently with these activities, we continued to:
- update the Calorimeter Trigger Readout and Control System User Requirements;
- update the system logical model;
- update the system architecture model.

2. Proposed Program

Our plan for the year 2001 is the following:

Oct. 2000 - Dec. 2000: Design, implementation, integration and test of the control and data transmission software for the Calorimeter Trigger Readout and Control System. The outcome of this phase should be a remote controlled single crate, Calorimeter Trigger Readout and Control System.

Oct. 2000 - Dec. 2000: Design, implementation and test of software for the Data Concentrator Card.

Oct. 2000 - Dec. 2000: Update of the CMS Calorimeter Trigger Readout and Control System User Requirements Document.

Dec. 2000: Release of the CMS Calorimeter Trigger Readout and Control System User Requirements Document first edition.

Jan. 2001 - Mar. 2001: Design, implementation and test of software for the Calorimeter Regional Trigger hardware, depending on the availability of Regional Trigger hardware prototypes. Alternatively we can design, implement and test the software for the rest of the Front-end Calorimeter Trigger hardware components should a fully configured ECAL Trigger hardware prototype be available instead.

Mar. 2001 - May. 2001: Update of the Calorimeter Trigger Readout and Control System logical model. Edition of the Calorimeter Trigger Readout and Control System Software Requirements Specification Document. Update of the Calorimeter Trigger Readout and Control System architecture model. Draft edition of the Calorimeter Trigger Readout and Control System Software Design Document.

Mar. 2001: Implementation and test of a standalone Calorimeter Trigger Readout and Control System version including a single (or dual) crate Front-end Sub-system and a single crate Regional Trigger Sub-system. This phase depends on a previous one and therefore is subject to change.

Apr. 2001: At CERN integration of the Calorimeter Trigger Readout and Control Front-end Sub-system software with the H4 Pre-calibration Test Beam System software.

May. 2001: At CERN system test of the Calorimeter Trigger Readout and Control Front-end Sub-system software with the H4 Pre-calibration Test Beam System software.

Jul. 2001: Participation in the Pre-calibration of the first CMS ECAL Super-modules in the H4 beam line.

Aug. 2001 - Dec. 2001: Design, implementation and test of either the software for the Calorimeter Regional Trigger hardware or the software for the rest of the Front-end Calorimeter Trigger hardware components depending on the availability of the hardware.

3. Resources

For the next 2001 calendar year we request financial support for software license renewals, and for the acquisition of additional hardware items and software licenses in order to complement the development environment that we have been installing at LIP-Lisbon.

An additional financial support is requested for the beginning of Q1 2001to acquire new hardware and software items for installing a similar development environment at CERN. This environment is essential for continuing:
- the integration and test at CERN of the hardware prototypes;
- our participation in the Pre-calibration of the first CMS ECAL Super-modules.

Sub-Project 5

QUALITY CONTROL

in the CMS Calorimeter Trigger and ECAL Readout Systems

Institutions:

- INESC, by means of two R&D Groups:
  - Instrumentation, Test and Packaging Group (ITPG)
  - Quality, Test and Hw/Sw Co-Design Group (QTHS)
- LIP-Lisbon

1. Project Status

The calorimeter trigger is a hierarchical system composed by hundreds of boards of the sub-systems Calorimeter Readout / Trigger Primitive Generator, Regional Trigger and Global Trigger distributed on tens of crates using a VME interconnection bus. Therefore, the complexity of the design and implementation of such a system makes the use of Design for Testability (DFT) techniques mandatory, in order to achieve a testable system during all the phases of the product production and lifetime.

During this year of 2000, INESC has developed one boundary scan controller board prototype, housed in the VME crate, intended to use the ANSI IEEE 1149.1 Standard (Boundary Scan - BS) to test the system at different levels. The corresponding software to perform the format translation needed to download the test stimuli and to recover the test response was also developed. This software establish a bi-directional link between the SVF format, generated by the commercial boundary scan software package VICTORY™, and the VME controller.

System-level modelling and specification using real-time, object-oriented modelling techniques have been used with the ECAL Front-End and Trigger Primitive Generators. A common CASE (Computer-Aided Software Engineering) platform is being used by LIP and INESC both for hardware and software model representation – Rationale-RT. Research has also been performed on valued characteristics and metrics for quality assessment of architectural solutions. The system-level modelling work is a critical factor of success for system integration and will become more significant in 2001.

The introduction of BIST in system ASICs, namely in the Tx_Rx synchronization IC, under development by TECMIC, has been implemented in a standard cell layout style, while TECMIC produced a alpha-version of a prototype Xilinx FPGA, tested at CERN (SubProject 1). Close cooperation between INESC QTHS Group, LIP and TECMIC is now a reality.

Test effectiveness validation, for classic single Line Stuck-At (LSA) and more realistic (defect-oriented) fault models is under way for the current structural description of the Sync Tx_Rx chip. Results show the usefulness of the approach, highlighting the need to verify how far pseudo-random test sequences, generated on-chip in the BIST solution, are able to uncover likely physical defects, and eventually the need to enhance the test pattern. Moreover, the design and test decisions on a possible, final FPGA-based product, incorporating two Sync Tx_Rx circuits, will be addressed during 2001, as a final decision has to be made by the end of next year.

2. Proposed Program

2.1 Application of Boundary Scan at System Level

Responsible: Instrumentation, Test and Packaging Group (ITPG)

This task addresses different aspects of the boundary scan test aimed to be used in all the phases of the experiment: prototyping, production and maintenance. During 2000 a prototype of the VME based boundary scan controller board was built and the development of the software for downloading the test and for sending back to the controller the test results will be concluded until the end of the year.

The main objective of this task is to redesign the JTAG module in order to make a portable module to be used in each DCC board, thus enabling the application of a boundary scan test to the sub-system during the idle time, or when a maintenance operation is required. The redesign of this board should lead to a

robust and reliable circuit and simultaneously take into account production problems, like cost, technologies used for the components and for the interconnection and intermediate and final tests.

This task has three components:
1. Redesign of the boundary scan test module into a portable module to be reused in different cards;
2. Development of the software implementing the bidirectional link between the SVF format generated by the commercial BS software package recently adopted by CERN and the VME BS controller;
3. Evaluation of the production constraints related with this board.

Due to changes in the constitution of the actual ITPG Group, this task will require the continuation of a close co-operation between LIP (involved in 2.1.1 and 2.1.2), INESC (involved in 2.1.3) and CERN, where all the experiment prototypes will be implemented.

2.2 System Modelling and Simulation

Responsible: QTHS (INESC)

As mentioned previously, in order to guarantee that the entire functionality of the system under development, as well as the required performance, is taken into consideration at the specification phase, a model, at system level, of its constituting modules or units, has to be developed and simulated. This need comes from the fact, that it is not possible to prototype all modules and interfaces of such a complex system. Thus, the use of system-level simulation is mandatory for achieving this purpose.

One of the key aspects that requires particular attention is the need to ensure the correct behavior, from functional and timing points of view, of the event builder block, within the ECAL DCC. In fact, unless timing constraints are met, data synchronization may be lost and consequently, the meaning of the received data and consequently its correct interpretation.

The purpose of this task is to pursue the work on system-level modeling and simulation of the ECAL read-out chain, putting emphasis on the validation of the event builder design and communication protocols. For that, Rational ROSE RT (Real Time) will be used to carry out modeling and simulation purposes. It will allow the animation of the constituting processes, in order to verify that the dynamic behavior of modules and interfaces will be correctly described in the specification. Such simulation process will also assist the design team in assigning the entire functionality among the different system components, performing a trade-off analysis in terms of the performance obtained with the different solutions. Finally, protocol test will be carried out. Constraints imposed by the already constructed modules will be considered during the modeling of the interfaces, and consequently in the simulation process.

This work will provide feedback to the design team, in order to allow in time correction of unforeseen errors.

2.3 ASIC BIST, Test Effectiveness and Reliability

Responsible: QTHS (INESC)

During 2000, a standard-cell implementation of the Sync Tx_Rx has been developed in CMOS AMS 0.35 µm technology, and using a proprietary standard cell library, IDLib0.35. Moreover, a close cooperation with TECMIC has been carried out to support the BIST implementation in the TECMIC Xilinx prototype of the Sync Tx_Rx chip. However, there has been several modifications in the context and specification of the syncronization chip (Sync Tx_Rx) under development by TECMIC, with the close cooperation of LIP and the INESC QTHS group. In fact, there is a trend towards the usefulness of having a single product with two embedded Sync systems, to be used both for the ECAL and the HCAL sub-projects. Moreover, technology and market evolution is making more cost-effective (and, thus, attractive) a FPGA final implementation. Therefore, this task has two main objectives for 2001:

1. To develop the final BIST solution for a 2-Sync Tx/Rx, single chip ASIC, portable to a programmable device (FPGA) technology implementation, with low area overhead, low speed degradation and low power BIST application;
2. To define the BIST sessions and tests in order to guarantee a very low escape rate in production, and a valuable lifetime self test of the component, using a Defect-Oriented (DO) test strategy, and INESC proprietary tools. Effort will continue to encourage other partners developing ASICs for the Trigger system, namely CAEN, to use INESC expertise, methodology and tools. Moreover, FPGA power

consumption, during BIST operation, will be investigated, with the aim of guiding the technology selection (vendor, FPGA family and target solution) for the final product.

DO test validation, and ASIC reliability will be addressed to derive high-quality tests, capable of uncovering physical defects, likely to occur during production or field use.

3. Resources

INESC will use its Lisbon infrastructure, namely its Laboratories for ASIC and Board Test and computer network, as well as a set of test software already available. Furthermore, some additional computing facilities (moderate) and advanced software packages will be required, namely in the domains of CASE tools and boundary scan packages at system level.

As human resources, INESC will use the expertise of five senior researchers, two Ph.D. students, one production technician to cover the different aspects of the research project, namely overall strategy, methodologies, advanced research, and experimentation and testing.

Sub-Project 6

TEST BEAM ECAL MONITORING

Two senior members of the LIP/CMS group particpated during this year in the development of the monitoring system of the ECAL test beam setup. The ECAL barrel supermodules (structures with 1700 crystals) and the endcap Dees will be tested and calibrated in the H4 CERN electron beam during the next three years. 36 supermodules and 4 Dees will undergo this calibration process. A large experimental infrastructure, including readout electronics, data acquisition, trigger, cooling, test systems, etc. will be installed in the CERN North Area to allow the completion of this program. The size of this experimental setup is typical of any fixed target experiment. Many experimental aspects related to the physics behaviour of the CMS electromagnetic calorimeter will be studied in this environment.

The LIP/CMS group has a strategical interest in the participation of this test beam program since it will provide a very good environment to train young physicists. On the other hand, the development of the monitoring software is complementary to other elements of our project (hardware modules, readout and control software) that will also be integrated in the test beam environment.

Sub-Project 7

PHYSICS RECONSTRUCTION AND SELECTION

During the following year, LIP will take part in a new CMS Project, called *Physics Reconstruction and Selection* (PRS), with the following scope:

- Simulation of detector signals
- Online reconstruction and physics selection
- Offline reconstruction
- Calibration of the detectors

LIP will contribute to the development and optimization of algorithms to be used in the CMS offline reconstruction and analysis. LIP will focus on the reconstruction of events containing electromagnetic objects, in particular combining the ECAL endcap data with that of a preshower detector in order to improve energy resolution. The performance of different algorithms will be studied and compared in terms of energy and position resolution, as well as efficiency, for different physics events.

LIP will also be involved in the development of techniques for online identification of electrons and photons by the CMS High Level Trigger system. This system consists of a large computer farm, running

real-time software, i.e. streamlined versions of the more sophisticated reconstruction packages used offline.

In parallel, LIP will investigate algorithms aimed at the reduction of first-level trigger rate in the ECAL endcap region, without loss of efficiency nor worsening of performance of this detector. These algorithms, based in energy distributions per groups of crystals and isolation criteria, should be simple enough that they can be easily implemented in hardware.

All these algorithms will be integrated in the simulation, reconstruction and data analysis software of the CMS collaboration. This software is a complex package, based on object oriented techniques which is currently under development and prototyping.

At a later stage, the performance of these selection and reconstruction tools will be evaluated by means of test-beam data, collected with a fully instrumented prototype of the electromagnetic calorimeter, including readout and trigger chain.

RESULTS FROM PREVIOUS PROJECTS

Projects with participation of LIP members:

1994
Financing agency: JNICT
Project reference: STRDC/C/FAE/1011/93
Financing: 14600 contos
Dates: 1/1/94 to 31/12/94
Title: Neural Methods in High Energy Physics
Participants (signing this proposal): J. Varela, P. Bordalo, S. Ramos

Summary: Research on algorithms, architectures and neural methods adapted to high energy physics problems, with particular emphasis on the trigger systems of the future LHC experiments. Study of the calorimeter trigger of the CMS experiment. Study of the trigger of the Squash experiment. Beam tests of the electromagnetic calorimeter Shashlik.

Publications:

The Compact Muon Solenoid (CMS), Technical proposal', CERN/LHCC 94-38

Calorimeter trigger in CMS: algorithm studies, Ph. Busson, J. Varela, CMS technical note 94-219, 1994.

Influence of dead materials and cracks in the performance of the CMS e.m. calorimeter, V. Genchev, V. Popov, J. Varela, CMS technical note 94-176, 1994.

New test beam results of Shashlik and preshower prototypes, J. Badier et al., CMS technical note 94-152, 1994.

Multi-bundle Shashlik calorimeter prototypes: beam-test results, J. Badier et al., CMS technical note 94-197, 1994.

Status report: Embedded architectures for second level triggering, RD11 Collaboration, CERN-DRDC-94-20, 1994.

Multibundle shashlik calorimeter prototypes beam test results, RD36 Collaboration (J. Badier et al.). 1995. Nucl. Instrum. Methods A354 (1995) 328-337.

Strangelet, quark and antinuclei search at high sensitivity,
Proposal SPSLC/P289, CERN/SPSLC 95-15, 1995.

1995
Financing agency: JNICT
Project reference: PCERN/P/FAE/130/94
Financing: 31500 contos
Dates: 1/1/95 to 31/12/95
Title: R&D on Calorimeter Trigger Systems
Participants (signing this proposal): J. Varela, P. Bordalo, S. Ramos, S. Silva, J.C. Silva, J. Gomes

Summary:
Study of the calorimeter trigger of the CMS experiment and study of the trigger of the Squash experiment.

Study of trigger algorithms:
During 95, the LIP group developed a study based on a more complete simulation, using the CERN software packages Pythia (event generator) and Geant (detector simulation). A detailed description of the CMS detector implemented in the CMSIM package was used, and a method which combines the Geant hadronic shower description with a parametrization of the electron showers was developed.
In 1995, the portuguese group proposed an improved version of the trigger algorithms, known as 'fine grain trigger', which combines the good features of the previous algorithms and which takes profit of the fine granularity of the e.m. crystal calorimeter.

System design
Encouraged by the results of the study of the 'fine grain' trigger, we decided to investigate in 95-96 the engineering feasibility of this concept. This implied the investigation of the fine grain trigger primitive generation close to the front-end and the study of the implications of the new primitives on

the Regional Crate backplane and on the Processor Card. The first aspect was studied by the portuguese group together with LPNHE-Palaiseau.

Development of prototypes
The LIP group, together with LPNHE-Palaiseau and the CMS calorimeter electronics group, developed an integrated prototype of the front-end calorimeter electronics, trigger primitive generator and optical transmission, and test, control and readout functions. Design work was performed during 1995.

Publications:
Physics at the Large Hadron Collider,
J. Varela, in Proceedings of the 'XV Autumn School', Nuclear Physics B (Proc. Suppl.) 37C (1995) 121-134, Lisbon, 1993
A contribution for the trigger strategy of CMS,
C. Lourenço, J. Varela, CMS technical note 95-025, 1995.
Towards a fine granularity calorimeter trigger for CMS,
C. Lourenço, J. Varela, CMS technical note 95-027, 1995.
A low Pt 1st level single electron trigger for beauty studies in CMS,
C. Lourenço, A. Nikitenko, J. Varela, CMS TN 95-197, 1995.
A study of the 1st level t trigger,
A. Nikitenko, J. Varela, CMS TN 95-195, 1995.
A simulation study of the ECAL/HCAL interface region,
A. Nikitenko, J. Varela, CMS TN 95-196, 1995.
A neural network trigger with a RICH detector,
R. Nóbrega, J. Varela, in Proceedings of '4th International Workshop on Software Engineering and Artificial Intelligence for High Energy and Nuclear Physics, Pisa, 1995.
A RICH counter for trigger and detection of exotic particles,
R. Nóbrega, P. Sonderegger, J. Varela, in Proceedings of 'RICH95 Workshop', Upsala, 1995.
Requirements for a fine grain calorimeter trigger,
J. Varela, in Proceedings of 'First Workshop on Electronics for LHC Experiments', Lisbon, 1995.
Beam test results of a shashlik calorimeter in high magnetic field,
RD36 Collaboration (P. Aspell et al.). CERN-PPE-95-152, Sep 1995. 20pp. , Nucl.Instrum. Methods

1996
Financing agency: JNICT
Project reference: PCERN/P/FAE/1033/95
Financing: 42100 contos
Dates: 1/1/96 to 31/12/96
Title: Participation in the CMS/LHC experiment (Development of the Calorimeter Trigger System)
Participants (signing this proposal): J. Varela, P. Bordalo, S. Ramos, S. Silva, J.C. Silva, J. Gomes

Summary:
Development of the calorimeter trigger of the CMS experiment
A significant contribution to *the simulation study of the trigger algorithms* was done in 1996.
In 1996 the main milestone (CMS Trigger/DAQ milestone D21) was *the test of a Trigger Primitive Prototype System,* in conjunction with the ECAL FERMI electronics prototype, and with the crystal calorimeter prototype in the H4 beam. This milestone was successfully completed.
The *design of the trigger control system* was pursued according to the schedule. During 1996 we pursued the definition of the control and readout model, which in this phase was translated in a rather extensive User Requirements Document. The first release of the document was submitted to comments by the collaboration in October 1996.
In 1996, the LIP group developed a conceptual design the *trigger data synchronization system.*
In the software area an activity on the evaluation of object-oriented design methods and tools, object-oriented data-bases and on the use of the CORBA standard in control systems was foreseen. A collaboration with the portuguese software company OBLOG was also planned. These activities were severely suppressed or postponed due to lack of resources.

Publications:
Energy and spatial resolution of a shashlik calorimeter and a silicon preshower detector,
RD36 Collaboration (P. Aspell et al.). CERN-PPE-95-151, Sep 1995. 34pp.

Nucl. Instrum. Methods A376:17-28, 1996
CMS electron/photon trigger - A simulation study with CMSIM data,
R. Nóbrega, J. Varela, CMS TN 96-21, 1996.
Preliminary specifications of the baseline trigger algorithms,
CMS Calorimeter Trigger Group, CMS-TN-96-10, 1996
Hermetic EM Calorimetry in CMS,
R. Ribeiro, J. Varela, CMS-TN-96-64, 1996
Second level e/γ calorimetr trigger in CMS,
R. Nóbrega, J. Varela, CMS NOTE 1996/010.
CMS Calorimeter Trigger Primitives Boards,
Ph. Busson, D. Lecouturier, E. Machado, P. Matricon, J.C. Silva, J. Varela,
CMS IN 1996/008
A method for synchronization of the trigger data,
J. Varela, CMS NOTE/1996-011
A Compression Scheme for ECAL Trigger Primitives,
Ph. Busson, R. Nobrega, J. Varela, CMS IN 1996/007

1997
Financing agency: JNICT
Project reference: PCERN/C/FAE/1106/96
Financing: 30000 contos
Dates: 1/1/97 to 31/12/97
Title: Participation in the CMS/LHC experiment (Development of the Calorimeter Trigger System)
Participants (signing this proposal): J. Varela, P. Bordalo, S. Ramos, S. Silva, J.C. Silva, J. Gomes

Summary:
The LIP research activities in CMS in 1997 had four main components: i)analysis of test beam data collected with the trigger prototypes; ii) development of trigger data synchronization prototypes; iii) design of the trigger readout & control system; iv) development of high level trigger algorithms.

Trigger prototypes and analysis of test beam data

The analysis, performed by the LIP group, of the data collected in June-August 96 in the H4 test beam with a prototype of the trigger and digital processing electronics for the electromagnetic calorimeter of the CMS experiment, coupled to a prototype of the PbWO4 crystal calorimeter, was concluded. The good quality of these data shows that the system performed as expected. A very successful operation was achieved for this system, which runs in synchronous and pipelined mode at the LHC clock frequency, and performs the basic trigger and data acquisition functions needed in the CMS electromagnetic calorimeter. The performance of the trigger front-end electronics is well within the established requirements: a highly efficient bunch crossing identification (>99.9%), a good trigger energy resolution ($\sigma=9\%/\sqrt{E}\oplus 2\%$) and a highly efficient electron cluster shape identification (99%) have been achieved. The FERMI digitizing system based on a dynamic analog compressor and a sampling ADC showed a very good performance, in particular the energy resolution for 150 GeV electrons was 0.54%, equal to the resolution obtained with a conventional charge integration ADC system.

Trigger data synchronization prototypes

The LIP group developed the method to synchronize the trigger data, transmitted through the 4000 optical links, at the input of the regional trigger processors (CMS Note 1996/011 'A method for synchronization of the trigger data'). A specification of the basic components, the Sync TX and Sync RX circuits, was produced ('Specification of the prototype trigger synchronization Tx/Rx circuits', CMS IN 1997/009). The design of this circuits was undertaken by the portuguese enterprise Tecnologias de Microelectronica (TECMIC). This circuits were integrated in the trigger synchronization test setup and were successfully tested.

Design of the trigger readout & control system

The basic object-oriented tools necessary to the development of a small scale prototype were installed, namely the Rational/Rose C++ CASE system and the object oriented data base Objectivity.

High-level trigger algorithms

The study of the 2nd level electron/photon trigger was concluded. Using the full granularity of the e.m. calorimeter and a dedicated neural network algorithm, the electron/photon trigger rate is reduced by a factor 7 keeping the electron/photon efficiency at 98%.

This work is part of a research line in neural networks applied to high energy physics initiated by the group in 1992. The writing of a PhD thesis on the area of neural networks applied to triggers in HEP was concluded.

Publications:

Modular Neural Networks applied to trigger in high energy physics,
Ph. Busson, R. Nóbrega, J. Varela, Nucl. Instrum. Meth. A 410 (1998) 273-283
Beam tests of the trigger and digital processing electronics for the electromagnetic calorimeter of the CMS experiment.,
R. Benetta et al. Nucl. Instrum. Meth. A 413 (1998) 31-42.
Neural Networks in HEP triggers
R. Nobrega, J.Varela, published in the proceedings of 'Computing for High Energy Physics', Berlin, April 1997.
Trigger Synchronisation Circuits in CMS,
J. Varela, in Proceedings of 'Third Workshop on Electronics for LHC Experiments', London, 1997.
Specifications of the prototype trigger synchronization Tx/Rx circuits,
J.C. Silva, J. Varela, CMS IN 1997/009
The TPB System Board Technical Documentation,
A. Almeida, E. Machado, R. Nobrega, J.C. Silva, J. Varela, CMS IN 1997/013
ECAL data volume,
R. Benetta, Ph. Busson, B. Lofstedt, M. Hansen, R. Nóbrega, J.C. Silva, J. Varela,
CMS NOTE 1997/059
Trigger Synchronisation Circuits in CMS
J. Varela, L. Berger, R. Nobrega, A. Pierce, J.C. Silva
CMS CR/1997 - 017

1998

Financing agency: FCT
Project reference: PCERN/P/FAE/1147/97
Financing: 40000 contos
Dates: 1/1/98 to 31/12/98
Title: CMS/LHC Experiment at CERN: Collaboration in the Development of the Calorimeter Trigger System
Participants (signing this proposal): J. Varela, P. Bordalo, S. Ramos, S. Silva, J.C. Silva, J. Gomes, A. Almeida, J.P. Teixeira, I.C. Teixeira.

Summary:

A redefinition of the Trigger Primitive Generation (TPG) architecture was produced reflecting the need to increase the flexibility of the trigger algorithms and the need to integrate the TPG with the calorimeter readout functions. The final partition of responsibilities between the institution involved in the ECAL trigger and readout system was defined. A study of a Neural approach for the e/γ trigger primitive generation was made showing a potential reduction of the e/γ trigger rate by a factor 4.

The functionality and technical choices for the prototype Local Readout Unit (LRU) in the trigger crates were identified. The engineering design of the LRU/PMC prototype was done and the first prototypes were built. A first release of the Ecal DCC System Design Description document was produced.

The develop of a first prototype of the Calorimeter Trigger Read-out and Control System software was started, including the functionality needed to operate the Trigger Primitives System hardware prototypes.

During the first year of the collaboration, INESC has been evaluating the use of the ANSI IEEE 1149.1 Standard at different levels (component, MCM, board, system), the inclusion of self-test techniques, in-system test procedures, as well as, the specification of the system using a high level description approach.

Publications:

Calorimeter Trigger Primitives, System Requirements Specification, edited by J. Varela, TriDAS/CT/TPS/SRS/2.0/1.0, 12 May 1998.
Study of a Neural Approach for lower level e/γ calorimeter trigger in CMS, N. Leonardo, J. Varela, CMS NOTE 1998/081
ECAL Data Concentrator - System Design Description, J.C. Silva, C. Tully, J. Varela, G. Varner, Preliminary Specification, Draft 0.1, 4 June 1998, CMS Technical Document
DCP, A Data Communications Protocol framework for a HEP Data Acquisition System, Software Requirements Document, I. Videira, S. Silva, CARDS SRD-DCP-vDraft

CARDS Front-end Sub-system, Software Requirements Document, S. Silva, CARDS TPS-SRD-vDraft, CMS Technical Document
Using the Boundary Scan testing at System Level, N. Cardoso, INESC, March 1998
Proposed Methods for Testing a Board Composed of Several Modules, N. Cardoso, INESC, 1998.
Application of Boundary Scan at Board and System Level, N. Cardoso, C, Beltran, INESC, Intermediate Report of Task 4.2, Project Nº CERN/P/FAE/1147/97
Study of Rates from High-level Trigger of B0s Events, N. Leonardo, J. Varela, CMS NOTE 1998/082

Financing agency: FCT
Project reference: PCERN/P/FAE/1144/97
Financing: 6000 contos
Dates: 1/1/98 to 31/12/98
Title: Development of the CMS Trigger Synchronization ASIC.
Participants (signing this proposal): J. Varela, J.C. Silva, Luís Berger, Adrian Pierce.

Summary:
The specification of the second version of the synchronization circuit was written and the design was done at TECMIC. An implementation in FPGA was produced and tested.
The new Synchronization circuit was integrated in a prototype of the SLB (Synchronization and Link Board.
In parallel a new VME test board to evaluate the performance of the new circuit was developed.
As part of the quality control tasks developed by INESC, the circuit design was analyzed by the INESC group in order to include built-in self-test structures. The BIST was integrated in the FPGA version.

Publications:
Specifications of the Calorimeter Trigger Synchronization Circuit, Version 2.2, J. C. Silva, J. Varela, CMS Internal Note to be published.
Introduction of Built-In Self Test (BIST) in the Sync Tx/Rx IC, M. B. Santos, J. P. Teixeira, INESC, June 1998.
Using an LHC-like Test Beam to Study the Trigger and Front-End Readout Synchronization of the CMS Detector
J. Varela, CMS IN 1998-012

Financing agency: FCT
Project reference: PCERN/P/FAE/1152/97
Financing: 3500 contos
Dates: 1/1/98 to 31/12/98
Title: Development of the Alignment System of the CMS Inner Tracker
Participants (signing this proposal): J. Varela.

1999
Financing agency: FCT
Project reference: CERN/P/FIS/1193/98
Financing: 35000 contos
Dates: 1/1/99 to 31/12/99
Title: Collaboration in the CMS/LHC Experiment at CERN
Participants (signing this proposal): J. Varela, P. Bordalo, S. Ramos, S. Silva, J.C. Silva, J. Gomes, A. Almeida, J.P. Teixeira, I.C. Teixeira.

Summary:
The SLB prototype was successfully tested in a dedicated test system built on purpose. The SLB prototype includes all the functionality except the trigger links.
The concept of ECAL selective readout for reducing the amount of data to be collected without damaging the physics, developed by LIP, was simulated in order to estimate data volumes and impact on physics.
A study of selective readout implementations and an architectural design of the data collection were performed. Preliminary system simulations were done in order to estimate buffer sizes and readout latencies.
The design of the Trigger Control Software was pursued, in particular the calorimeters front-end software.

During the second year of the collaboration, INESC has been evaluating the use of the ANSI IEEE 1149.1 Standard (BoundaryScan) (BS) at different levels (component, MCM, board, system), the inclusion of self-test techniques in system test procedures, the validation of test effectiveness and system specification and simulation using a real-time object-oriented modeling technique.

Publications:

Recent developments in the CMS Calorimeter Trigger,
T. Monteiro and CMS ECAL Upper-Level Readout and Trigger group, to be published in Proceedings of Int. Conf. on Calorimetry in HEP (CALOR99) Lisbon (Portugal), 1999.

Selective Readout in the CMS ECAL
T. Monteiro, Ph. Busson, W. Lustermann, T. Monteiro, J. C. Silva, C. Tully, J. Varela,
in Proceedings of 'Fifth Workshop on Electronics for LHC Experiments', Snowmass, Colorado, USA, 1999.

Testability Issues In The CMS Ecal Upper-Level Readout And Trigger System,
Carlos Beltrán Almeida, Isabel Cacho Teixeira, Joao Paulo Teixeira, José Augusto, Marcelino Santos and Nuno Cardoso, INESC, Lisboa , Joao Varela, CERN Geneve/LIP Lisbon in Proceedings of 'Fifth Workshop on Electronics for LHC Experiments', Snowmass, Colorado, USA, 1999.

Study of the ECAL Data Concentrator,
C. Tully, J. Varela, J.C. Silva, G. Varner, CMS IN-1999/012

Techical Specifications of the ECAL trigger Synchronization and Link Board, S. Silva, J. Varela, CMS IN-2000/005

ECAL Data Synchronization, J. Varela et al., CMS IN-2000/006

Financing agency: FCT
Project reference: CERN/P/FIS/1192/98
Financing: 10000 contos
Dates: 1/1/99 to 31/12/99
Title: Development of the Alignment System of the CMS Inner Tracker
Participants (signing this proposal): J. Varela.

2000

Financing agency: FCT
Project reference: CERN/P/FIS/15170/99
Financing: 43000 contos
Dates: 1/1/00 to 31/12/00
Title: Collaboration in the CMS/LHC Experiment at CERN
Participants (signing this proposal): J. Varela, P. Bordalo, S. Ramos, S. Silva, J.C. Silva, J. Gomes, A. Almeida, J.P. Teixeira, I.C. Teixeira.

Financing agency: FCT
Project reference: CERN/P/FIS/15171/99
Financing: 6000 contos
Dates: 1/1/99 to 31/12/99
Title: Development of the Alignment System of the CMS Inner Tracker
Participants (signing this proposal): J. Varela.

Projects with participation of INESC members:

1994
Financing Agency: ESPRIT II
Project Reference: ESPRIT 7802
Financing: 12069 contos
Dates: 22/06/93 to 21/06/94
Title: APBB Advanced Prom Building Blocks
Participants (Signing this proposal) I.M.C. Teixeira

Summary: The objective of the project was the development of a technology that integrate EEPROM with already existing (Plessey and SGS Thomson) technologies. Several Institutions and small companies joint the project in order to develop a set of demonstrators for the technology. INESC has used the technology for developing an Electronic Electric Power meter.

Reports:

Carlos Cruz, Carlos Pinto, João Barata, Isabel Teixeira, "ASIC for an Electronic Electric-Power Meter: Test Results", APBB Project Deliverable, December 1993.

Results:
The work carried out during the first part of this Project, that took place on the previous years, has been the basis for the 3 M.Sc.thesis. It has been, also, the basis for one Final Project, which has been awarded by the Portuguese Ordem dos Engenheiros with the 1st place on the "young engineer better work contest".

1995
Financing Agency: ESPRIT III
Project Reference: ESPRIT /OMI 9264
Financing: 15 000 contos
Dates: 03/01/93 to 28/02/95
Title: OSIM-AHS: Open and Scalable Intelligent Meter for Advanced Home Services
Participants (Signing this proposal) I.M.C. Teixeira

Summary: The OSIM-AHS project aimed at providing an OMI-compatible intelligent meter prototype capable of operating in the near-real user exploitation environment. The project included a feasibility study of its industrially significance and Pan-European R&D projects. Also, aimed at providing strategic information about the product concepts and corresponding markets to be served.

Publications:
Isabel Teixeira, "Software Tools", OSIM-AHS Workshop on Energy Management Systems, Session: Technology Assessment Standardization Trends, Oct. 1994.
Carlos Pinto, Isabel Teixeira, "Technology Assessment: Architecture Requirements for System", OSIM-AHS Project Deliverable (D2.1), Nov. 1994.
Carlos Pinto, Isabel Teixeira, "Technology Assessment: Application software", OSIM-AHS Project Deliverable (D2.4), Sept. 1994.

1995
Financing Agency: ESPRIT III
Project Reference: ESPRIT 7107
Financing: 47 000 contos
Dates: 24/07/92 to 22/10/95
Title: ARCHIMEDES, "Architectural Methodologies for Advanced Testing of VLSI Systems"
Participants (Signing this proposal) J.P.C. Teixeira, I.M.C. Teixeira, F.M.D. Gonçalves, M.B. Santos

Summary: Archimedes aimed at bridging the gap between to trends which are apparently antagonist in VLSI design: I) to design circuits from higher and higher levels in order to tae advantage of the very large number of devices authorised by the progress of the technology, ii) efficient testing must be based on IC defects fault models, which leads to non affordable times if testing is based on conventional test pattern generation for large design. Archimedes puts together experts on several individual testing methods, approaches and types in order to develop cross-fertilisation in view of a global solution.

Publications:

J.J.T. Sousa, F.M. Gonçalves, J.P.Teixeira, C. Marzocca, F. Corsi, T.W. Williams, "Defect Level Evaluation in an IC Design Environment", IEEE Trans. on CAD, vol. 15, nº. 10, pp. 1286-1293, 1996.
M. Dalpasso, M. Favalli, P. Olivo, J.P. Teixeira, "Realistic Testability Estimates for CMOS ICs", Electronics Letters, vol. 30. nº. 19, pp. 1593-1595, 15th September, 1994.
O.P. Dias, M. Calha, I.C. Teixeira, J.P. Teixeira, "High Level Specification for SFT using Object-Oriented Modeling Techniques", Proc. European Test Workshop (ETW), pp. 135, June, 1996
M. B. Santos, M. Simões, I. Teixeira, J.P. Teixeira, "Test Preparation for High Coverage of Physical Defects in CMOS Digital ICs", Proc. 13th IEEE VLSI Test Symposium (VTS), pp. 330-335, May, 1995.
C. Sebeke, J.P. Teixeira, M.J. Ohletz, "Automatic Fault Extraction and Simulation of Layout Realistic Faults for Integrated Analog Circuits", Proc. European Design and Test Conf. (EDTC), pp. 464-468, March 1995.
M. Calha, M. Santos, F. Gonçalves, I. Teixeira, J.P. Teixeira, "Back Annotation of Physical Defects into Gate-Level, Realistic Faults in Digital ICs", Proc. Int. Test Conference (ITC), pp. 720-728, Washington, D.C., Oct. 1994.
S. Hellebrand, J.P. Teixeira, H.-J. Wunderlich, "Synthesis for Testability - the Archimedes Approach", 1st International Test Synthesis Workshop, Santa Barbara, California, May, 1994.
J.J.T. Sousa, F.M. Gonçalves, J.P. Teixeira, T.W. Williams, "Fault Modeling and Defect Level Projections in Digital ICs", Proc. European Design and Test Conf. (EDTC), pp. 436-442, March, 1994.

1996

Financing Agency: JNICT
Project Reference: STRIDE/TIT/0067
Financing: 47467 contos
Dates: 01/07/93 to 30/06/96
Title: Electronic Systems for Electric Energy Measurement
Participants (Signing this proposal) I.M.C. Teixeira

Summary: The objective of the project was the development of a *fully integrated* electronic power meter, along with the study of feasibility of its production. Some experiments with FPGA should be carried out in order to study possible solutions.

Publications:
J.B. Barbosa, V.E. Antunes, I.C. Teixeira, "Offset Compensation in a Static Electric Current Meter", Proc. of Power and Timing Modeling for Performance of Integrated Circuits PATMOS'94, Barcelona, pp. 210-217, Setembro, 1994.

Deliverables:
J.Barbosa, V.Antunes, I. C. Teixeira, "Sistema de Medida para Telecontagem: sub-sistema analógico para contagem de energia electrica", Deliverable 1.B, July 95.
J.Barbosa, V.Antunes, I. C. Teixeira, "Sistema de Medida para Telecontagem: sistema de medida para contagem de energia electrica", Deliverable 2.B, July 95.

1996

Financing Agency: JNICT
Project Reference: STRIDE/C/TIT/93/92
Financing: 12500 contos
Dates: 14/01/94 to 14/01/96
Title: Quality and Test of Integrated Circuits
Participants (Signing this proposal) F. M. D. Gonçalves, M. B. Santos, J.P.C. Teixeira,

Summary: The purpose of this Project is to approach, in an integrated form, the area of *Quality and Test* of Integrated Circuits (ICs), and use the analysis of its physical testability as a vehicle to assess and improve, beyond the quality control of production process, its production yield and product reliability.

Publications:

F.M. Gonçalves, I.C. Teixeira, J.P. Teixeira, "Integrated Approach for Circuit and Fault Extraction of VLSI Circuits", Proc. of the IEEE Int. Symp. on Defect and Fault Tolerance in VLSI Systems, pp. 96-104, Boston, Ma., November, 1996.

P. Correia, P. Machado, P. Carvalho, M. Santos, F. Gonçalves, J.P. Teixeira, "Low Power CMOS Digital Cell Libraries: Performance and Testability", Proc. 6th. Int. Workshop on Power and Timing Modeling, Optimization and Simulation (PATMOS), Bologna, pp. 307-316, Sept., 1996.
F. Celeiro, L. Dias, J. Ferreira, M.B. Santos, J.P. Teixeira, "VHDL Fault Simulation for Defect-Oriented Test and Diagnosis of Digital ICs", Proc. EURODAC/EURO-VHDL, pp. 450-455, September, 1996.
F. Celeiro, L. Dias, J. Ferreira, M.B. Santos, J.P. Teixeira, "On VHDL Defect Modeling and Simulation in CMOS Integrated Circuits", Proc. European Test Workshop (ETW), pp. 227, June, 1996
M. B. Santos, M. Simões, I. Teixeira, J.P. Teixeira, "Test Preparation Methodology for High Coverage of Physical Defects in CMOS Digital ICs", Proc. European Design and Test Conf. (EDTC), pp. 604, March 1995.
M. B. Santos, J.P. Teixeira, "Self-Adaptive BIC Sensor for IDDQ Detection in Static CMOS Digital ICs", Proc. 4th. Int. Workshop on Power and Timing Modeling, Optimization and Simulation (PATMOS), pp. 218-225, Oct., 1994.

1996

Financing Agency: Esprit
Project Reference: Project EP 8374
Prime Contractor: Siemens Aktiengesellschaft; Partners: INESC, Dassault Electronique, Nederlands Philips Bedrijen B.V., Fraunhofer Einrichtung für Zuverlässigkeit und Mikrointegration (FhG/IZM), Thompson CSF, Institute für Mikroelectronik Stuttgart, Integrated Circuit Testing GmbH. Funding institutions: European Commission and the partners.
Financing: 2000000 ECU (For ITPG 160 000 ECU)
Dates: 3 years (November 1993 - November 1996).
Title: "LOCOP – Low Cost Packaging for Future Multi-Chip Solutions".
Participants (Signing this proposal) C.B.Almeida, J.S. Augusto

Summary: Within LOCOP a complete multi-chip packaging technology was developed, targeting to bring cost into the area of conventional SMD-mounted Printed Circuit Boards (PCBs) and even below. Several technology alternatives were explored: laminated substrates as well as ceramic substrates and active substrates; wire bonding and flip chip; completely encapsulated modules with a module package as well as non-encapsulated modules with encapsulated bare dies only. To demonstrate the benefits of developed technologies, to verify that the objectives were met and to quantify the improvements in cost, size and performance, several product demonstrators were designed and manufactured.

1996

Financing Agency: Esprit
Project Reference: Project EP 7502
Financing: 2 400 000 ECU (For ITPG 200 000 ECU)
Dates: 44 months (February 1993 - October 1996).
Title: "AIPAC - Advanced Interconnection Technology for Electronics"
Participants (Signing this proposal) C.B.Almeida, J.S. Augusto

Summary: AIPAC is not a R&D Project but an action aimed to increase the technological potential of Portuguese SMEs. The project, focused on Portuguese SMEs/SMIs, had as goals to increase the awareness in new high-density electronic packaging and interconnection technologies (COB, MCM, TAB), to make these technologies available to Portuguese SMEs, offering low-cost rapid prototyping and small series, to promote training actions on design methodologies and manufacturing aspects, and also to increase the awareness in using ASICs

1998

Financing Agency: JNICT
Project Reference: PRAXIS XXI 3/3.1/ENR/36/94
Financing: 41000 contos
Dates: 04/05/95 to 04/05/98
Title: Integrated Electronic System for the Evaluation and Intelligent Management of Domestic Consumption and Securitry
Participants (Signing this proposal) I.M.C. Teixeira

Summary: The main objective of the project was the specification and design of an hw/sw system that allow for the implementation of telecounting services. For that, the metrology, or electronic power meter was to be specified, as well as the communication platform. Communication systems should be studied in order to conclude about the feasibility of the different solutions, namely, the use of distribution power lines for transmission purposes. The information system behind the energy management system should be analyzed. Methodologies should be developed for dealing with such systems.

Deliverables:

Isabel Teixeira, Nuno Especial, "Análise e Especificação do Sistema Global", Deliverable D*.1, Dec. 1996
Joaquim Barbosa, Isabel Teixeira, "Arquitectura Preliminar do Módulo de Metrologia", Deliverable D2.2, March 1997.

Publications:

O.P. Dias, I.C. Teixeira, and J.P. Teixeira, “Metrics and Criteria for Quality Assessment of Testable Hw/Sw System Architectures”, accepted for publication at Journal of Electronic Testing, Theory and Application (JETTA), vol. 10, nº. 6, pp. , Kluwer Academic Publishers, 1998.
O.P. Dias, I.C. Teixeira, J.P. Teixeira, C.E. Pereira ,"Design and Quality Assessment of Real-Time Hw/Sw Systems Architectures", DCIS'98, pp. Nov., 1998.
O.P. Dias, I.C. Teixeira, J.P. Teixeira, C.E. Pereira , " Performance and Test Oriented Metrics and Criteria for Hw/Sw Design at System Level", ddces'98, pp. Poland, Set. 1998.
O.P. Dias, I.C. Teixeira, J.P. Teixeira, “Metrics for Quality Assessment of Testable Hw/Sw System Architectures”, Proc. European Test Workshop, May, 1998.
M. Calha, I.C. Teixeira, J.P. Teixeira, “OOM Approach for HW/SW Co-Analysis, Specification and Design of Heterogeneous Systems”, CESA IMACS Conf. (Computational Engineering in Systems Application), Lille, July, 1996.
O.P. Dias, M. Calha, I.C. Teixeira, J.P. Teixeira, “High Level Specification for SFT using Object-Oriented Modeling Techniques”, Proc. European Test Workshop (ETW), pp. 135, June, 1996
O.P. Dias, M. Calha, I.C. Teixeira, J.P. Teixeira, “HW/SW Specification Using OOM Techniques”, Proc. 7th. IEEE Int. Workshop on Rapid System Prototyping, June 1996.

PUBLICATIONS OF THE LIP/CMS GROUP
(Work related to the CMS project)

6.1. International journals

Multibundle shashlik calorimeter prototypes beam test results.
RD36 Collaboration (J. Badier et al.). 1995.
Nucl. Instrum. Methods A354 (1995) 328-337.

Beam test results of a shashlik calorimeter in high magnetic field,
RD36 Collaboration (P. Aspell et al.).
Nucl.Instrum. Methods A376: 361-367, 1996.

Energy and spatial resolution of a shashlik calorimeter and a silicon preshower detector,
RD36 Collaboration (P. Aspell et al.). CERN-PPE-95-151, Sep 1995. 34pp.
Nucl. Instrum. Methods A376:17-28, 1996

Modular Neural Networks applied to trigger in high energy physics,
Ph. Busson, R. Nóbrega, J. Varela,
Nucl. Instrum. Meth. A 410 (1998) 273-283

Beam tests of the trigger and digital processing electronics for the electromagnetic calorimeter of the CMS experiment.,
R. Benetta et al.
Nucl. Instrum. Meth. A 413 (1998) 31-42

A System Level Boundary Scan Controller Board for VME Applications, Nuno Cardoso, Carlos Beltrán Almeida, José Carlos Silva, submitted to Journal of Electronic Testing.

6.2. Published in proceedings of international conferences

Physics with the CMS Detector,
J.Varela, in Proceedings of 'International Workshop on Supersymmetry and Unification of Fundamental Interactions', Boston, Northeastern University, 1993.

Physics at the Large Hadron Collider,
J. Varela, in Proceedings of the 'XV Autumn School', Nuclear Physics B (Proc. Suppl.) 37C (1995) 121-134, Lisbon, 1993

A neural network trigger with a RICH detector,
R. Nóbrega, J. Varela, in Proceedings of '4th International Workshop on Software Engineering and Artificial Intelligence for High Energy and Nuclear Physics, Pisa, 1995.

A RICH counter for trigger and detection of exotic particles,
R. Nóbrega, P. Sonderegger, J. Varela, in Proceedings of 'RICH95 Workshop', Upsala, 1995.

Requirements for a fine grain calorimeter trigger,
J. Varela, in Proceedings of 'First Workshop on Electronics for LHC Experiments', Lisbon, 1995.

Neural Networks in HEP triggers
R. Nobrega, J.Varela, to be published in the proceedings of 'Computing for High Energy Physics', Berlin, April 1997.

Trigger synchronization circuits in CMS
L. Berger, R. Nóbrega, J.C. da Silva, J. Varela, submitted to the conference 'Electronics for LHC experiments', Oxford, Sept 97.

The CMS Calorimeter Trigger,
G.P. Heath et al., in Proceedings of 'Third Workshop on Electronics for LHC Experiments', London, 1997.

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T. Monteiro and CMS ECAL Upper-Level Readout and Trigger group, to be published in Proceedings of

Int. Conf. on Calorimetry in HEP (CALOR99) Lisbon (Portugal), 1999.

Testability Issues In The Cms Ecal Upper-Level Readout And Trigger System,
Carlos Beltrán Almeida, Isabel Cacho Teixeira, Joao Paulo Teixeira, José Augusto, Marcelino Santos and Nuno Cardoso, INESC, Lisboa , Joao Varela, CERN Geneve/LIP Lisbon,
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Selective Readout in the CMS ECAL
T. Monteiro, Ph. Busson, W. Lustermann, T. Monteiro, J. C. Silva, C. Tully, J. Varela,
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6.3. CERN Technical Notes

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J.Badier et al., CMS technical note 92-45, 1992.

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Light collection in the shashlik,
J.Varela, CMS technical note 93-71, 1993.

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RD11 Collaboration, CERN-DRDC-94-20, 1994.

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J.Badier et al., CMS technical note 94-152, 1994.

Influence of dead materials and cracks in the performance of the CMS e.m. calorimeter,
V. Genchev, V. Popov, J. Varela, CMS technical note 94-176, 1994.

New test beam results of Shashlik and preshower prototypes,
J. Badier et al., CMS technical note 94-152, 1994.

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J. Badier et al., CMS technical note 94-197, 1994.

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Ph. Busson, J. Varela, CMS technical note 94-219, 1994.

A contribution for the trigger strategy of CMS,
C. Lourenço, J. Varela, CMS technical note 95-025, 1995.

Towards a fine granularity calorimeter trigger for CMS,
C. Lourenço, J. Varela, CMS technical note 95-027, 1995.

A low Pt 1st level single electron trigger for beauty studies in CMS,
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A simulation study of the ECAL/HCAL interface region,
A. Nikitenko, J. Varela, CMS TN 95-196, 1995.

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R. Nóbrega, J. Varela, CMS TN 96-21, 1996.

Preliminary specifications of the baseline trigger algorithms,
CMS Calorimeter Trigger Group, CMS-TN-96-10, 1996

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Trigger Primitives Boards,
Ph. Busson, D. Lecouturier, E. Machado, P. Matricon, J.C. Silva, J. Varela,
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J. Varela, CMS NOTE/1996-011

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Ph. Busson, R. Nobrega, J. Varela, CMS IN 1996/007

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A. Almeida, E. Machado, R. Nobrega, J.C. Silva, J. Varela, CMS IN 1997/013

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R. Benetta, Ph. Busson, B. Lofstedt, M. Hansen, R. Nóbrega, J.C. Silva, J. Varela,
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C. Tully, J. Varela, J.C. Silva, G. Varner, CMS IN-1999/012

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ECAL Data Synchronization, J. Varela et al., CMS IN 2000/006