Electronics for the CMS ECAL Readout and Trigger

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LIP - Nov 2000

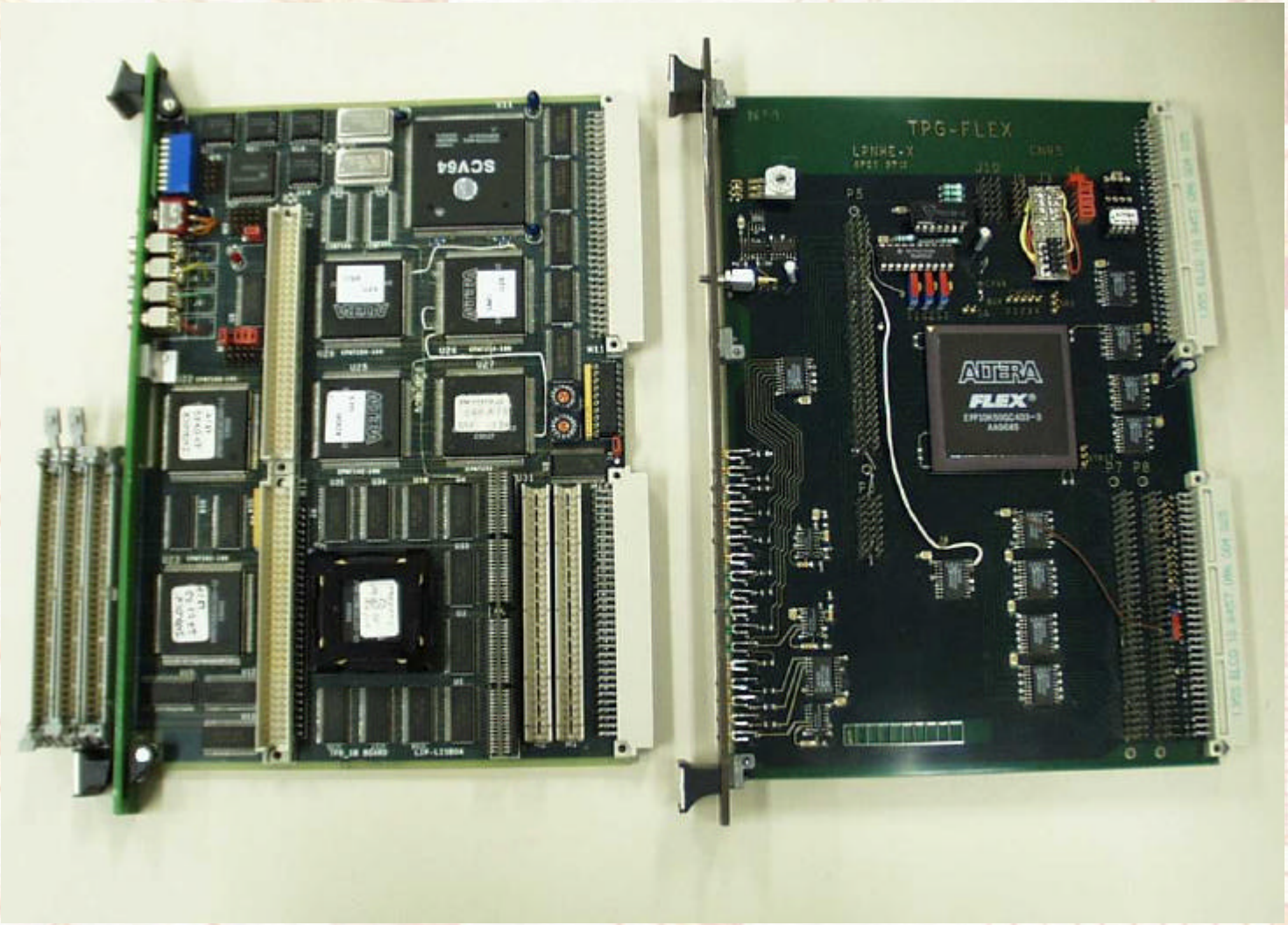
ECAL TPG algorithm

- CRP Study (1995)
- TPG prototype (1996-1998)
  - (SB + PB)
  - (SB + PB + SYNC BOARD)
  - (SB + PB + OB +TTC System + SYNC BOARD)

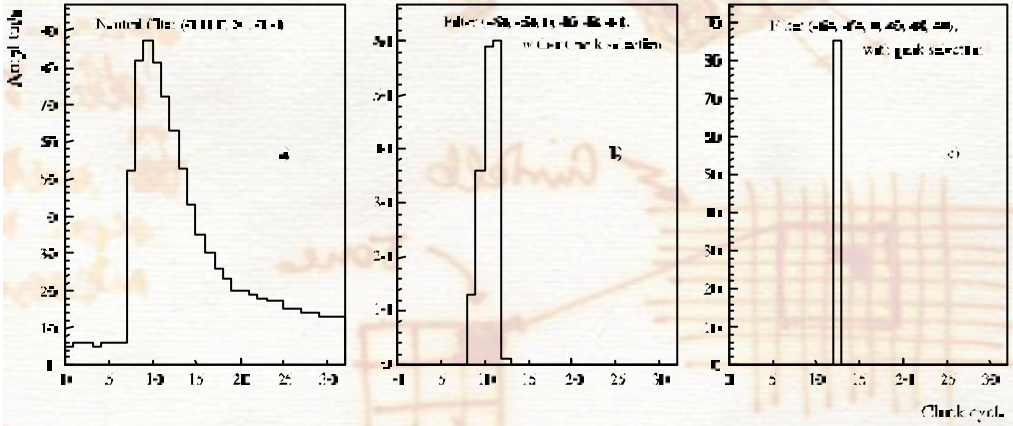
ECAL TPG proto SB-PB

- System Board (LIP)
  - 6 ch - 10 bits, 40 Mhz, Trigger data (32 samples) BS and Self-Test approach, DMA transfer, PB interface
- Processor Board (LPNHE-X)
  - L-Neuro 2
  - 6 ch 10 bits (8 + 2 @ 80 MHZ,
  - Sum OF 2, SUM MAX Address, Fine Grain Bit

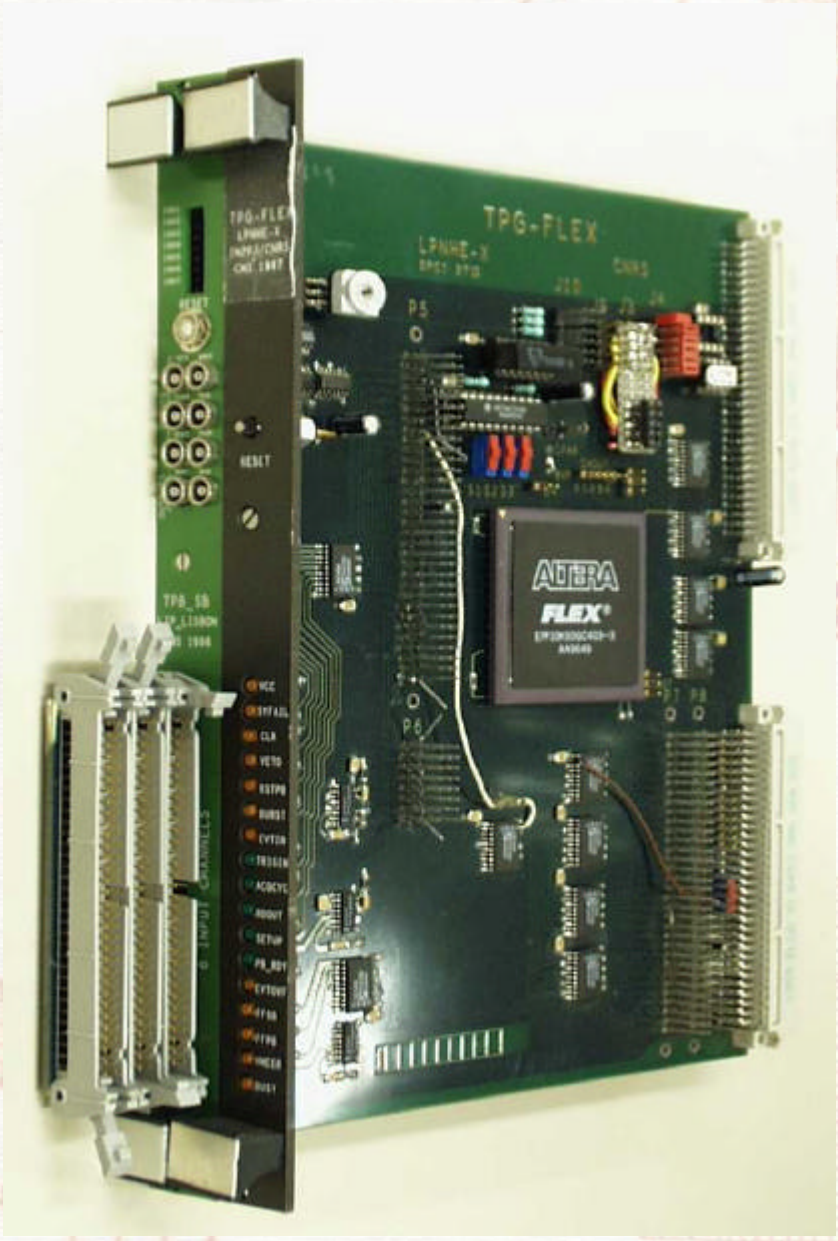
ECAL TPG proto
SB-PB



Beam test results:

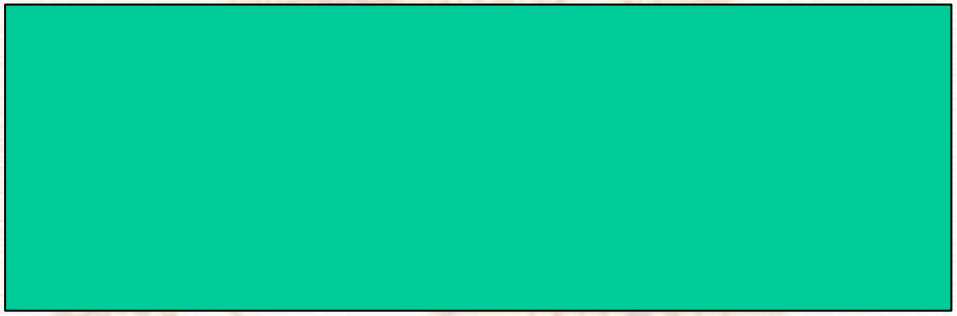


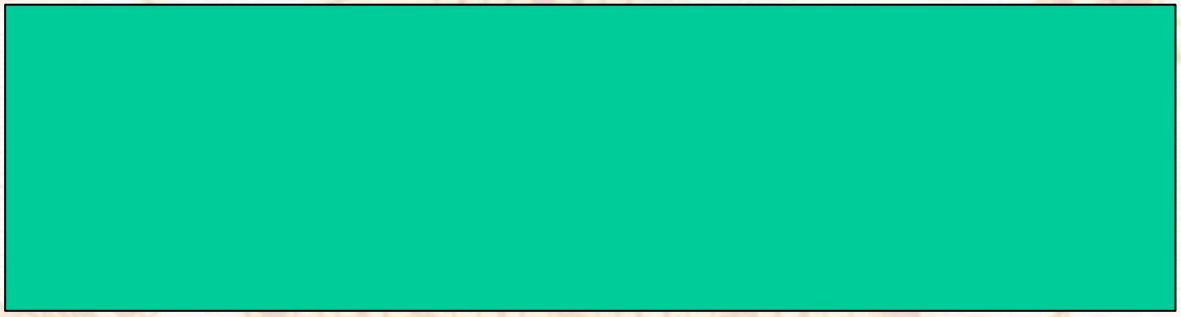
ECAL TPG
proto
SB-PB



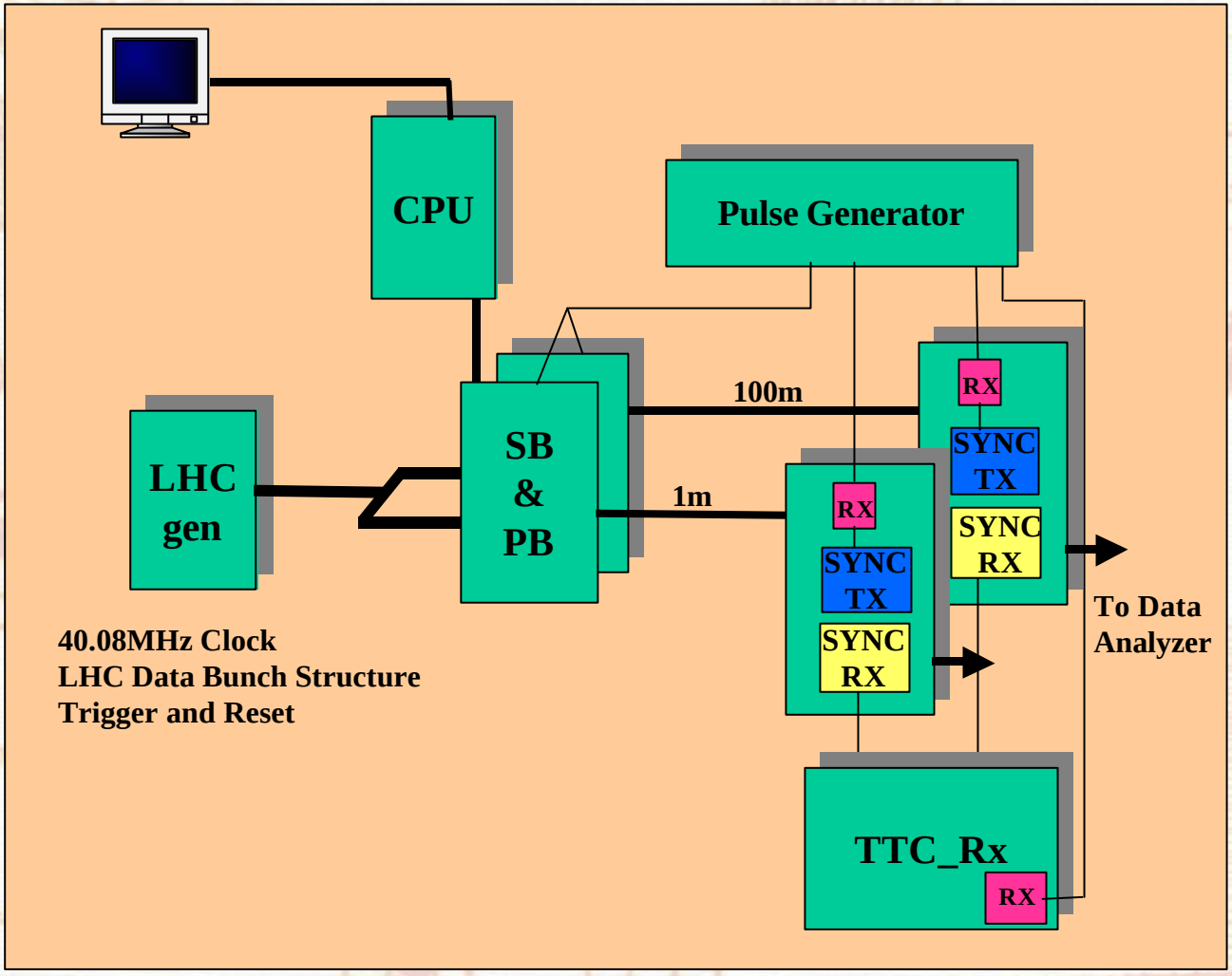
TPG and Synchronization

- TPG prototype (1996-1998)
  - (SB + PB + SYNC BOARD)

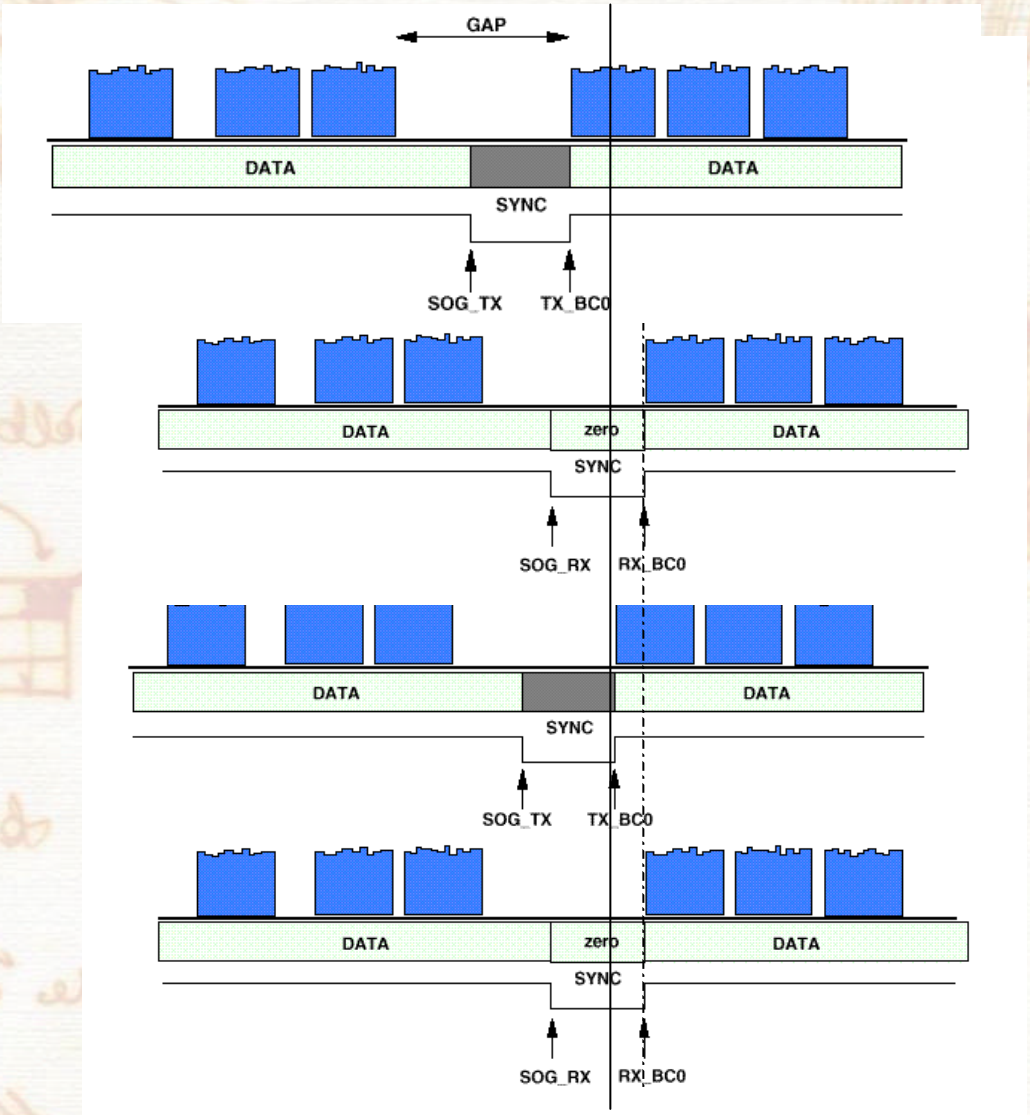




TPG and Synchronization



Synchronization FIFO



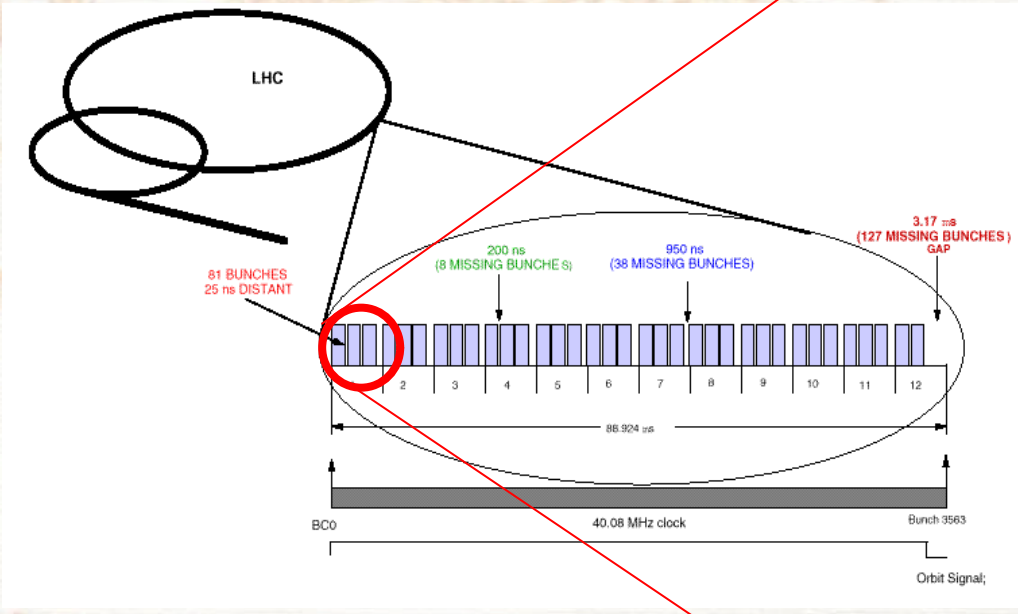
Ch#1 Input

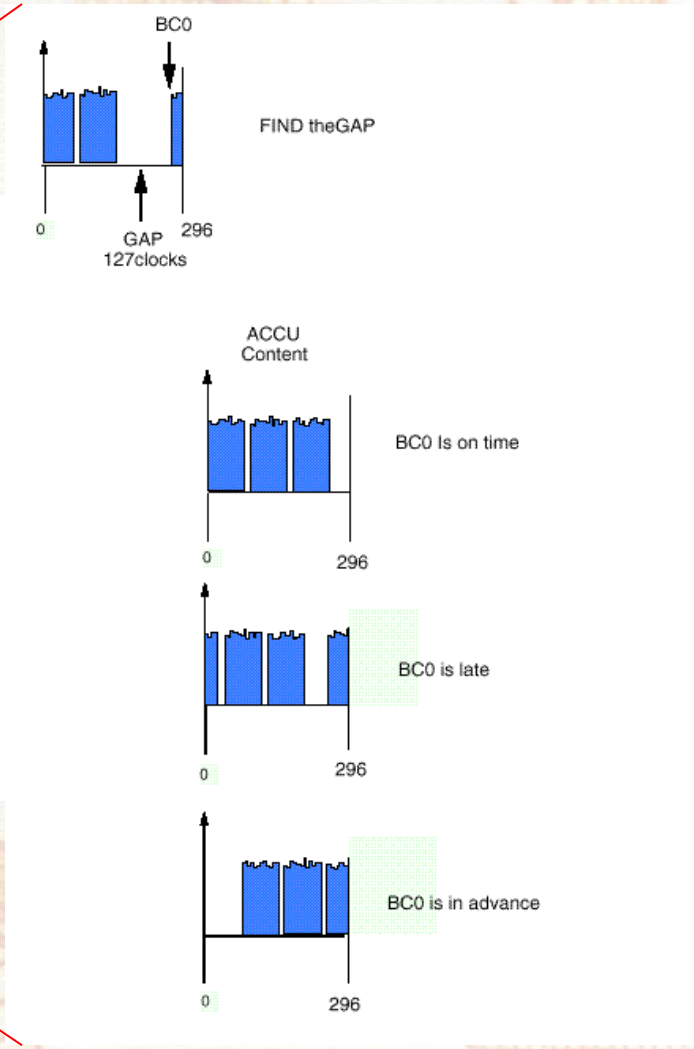
Ch#1 Output

Ch#2 Input

Ch#2 Output

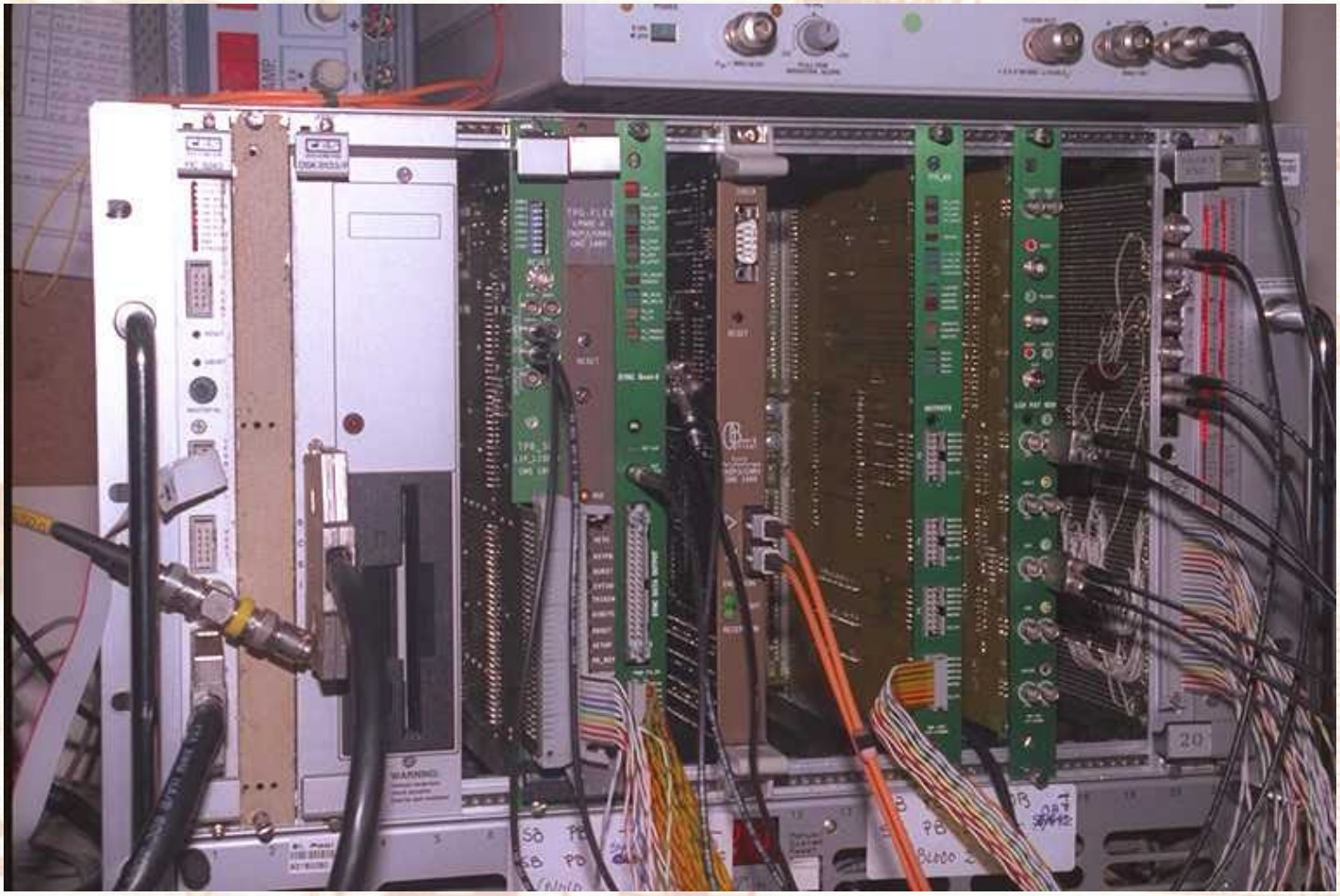
Alignment Histogram





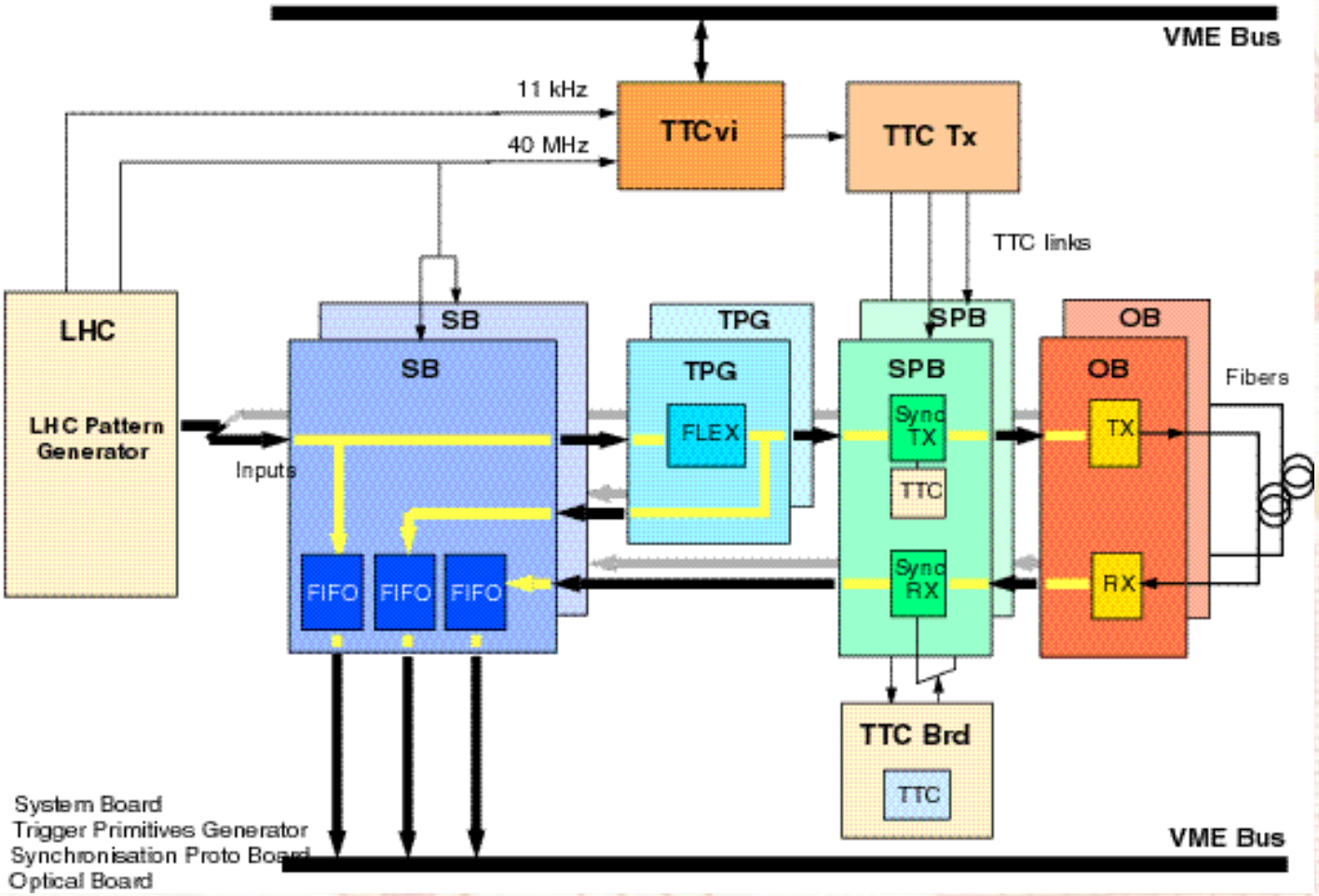
- **Adjust on the BC0 Time**

1997 test Bench



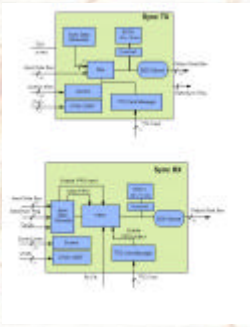
1998 test Bench

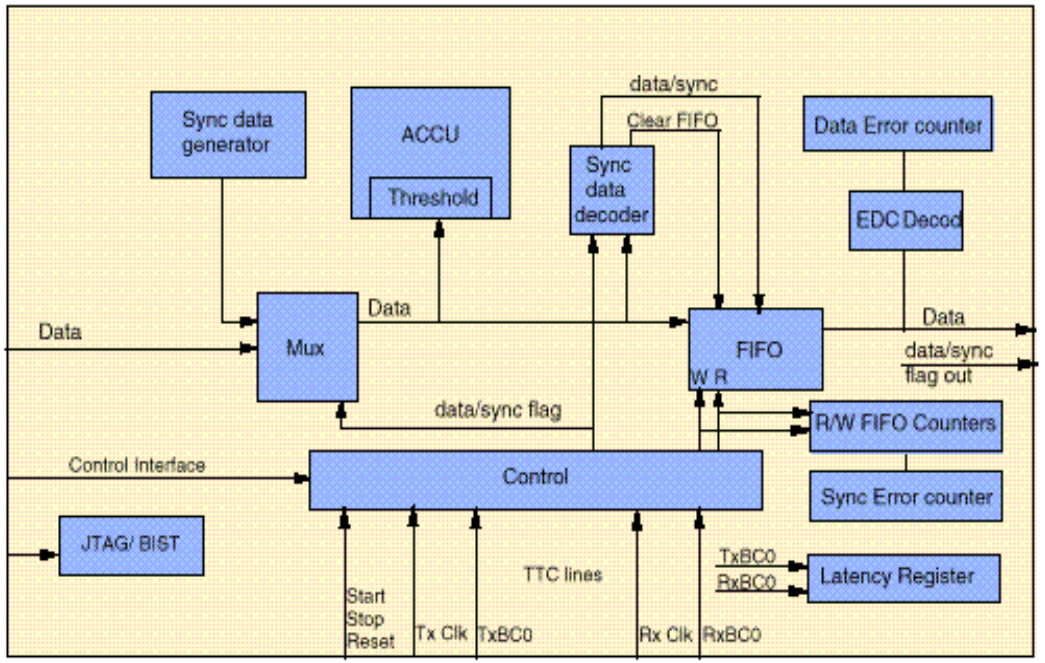
Trigger Synchronization Test Setup in 97



•(SB + PB + OB +TTC System + SYNC BOARD)

Sync TX-RX Block Diagram



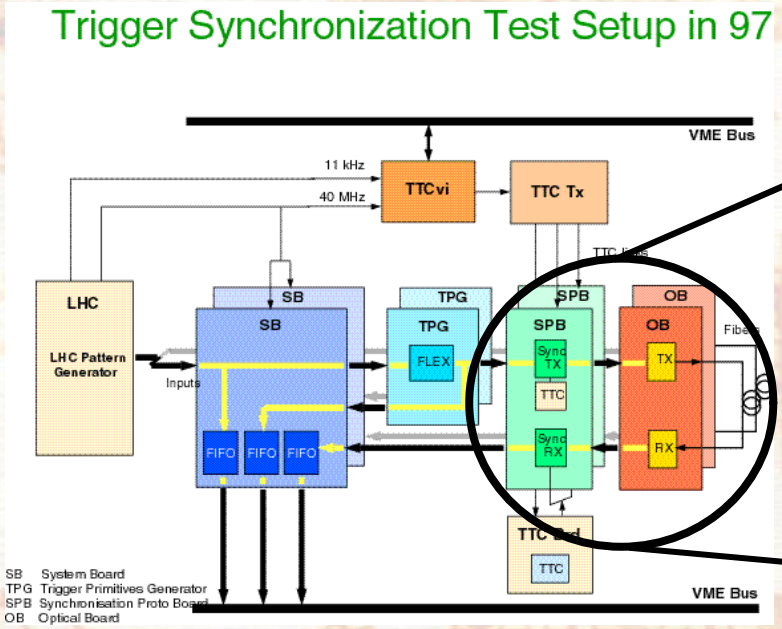


Differences from previous design:

- **Merge of the 2 circuits.**
- **24 Bits Data Bus.**
- **TTC Control Signals decoded on the BC.**
- **Internal Accumulator.**
- **FIFO Transparent Mode with programmable depth.**
- **Latency Register (Tx_BC0 > Rx_BC0 distance).**
- **BIST.**

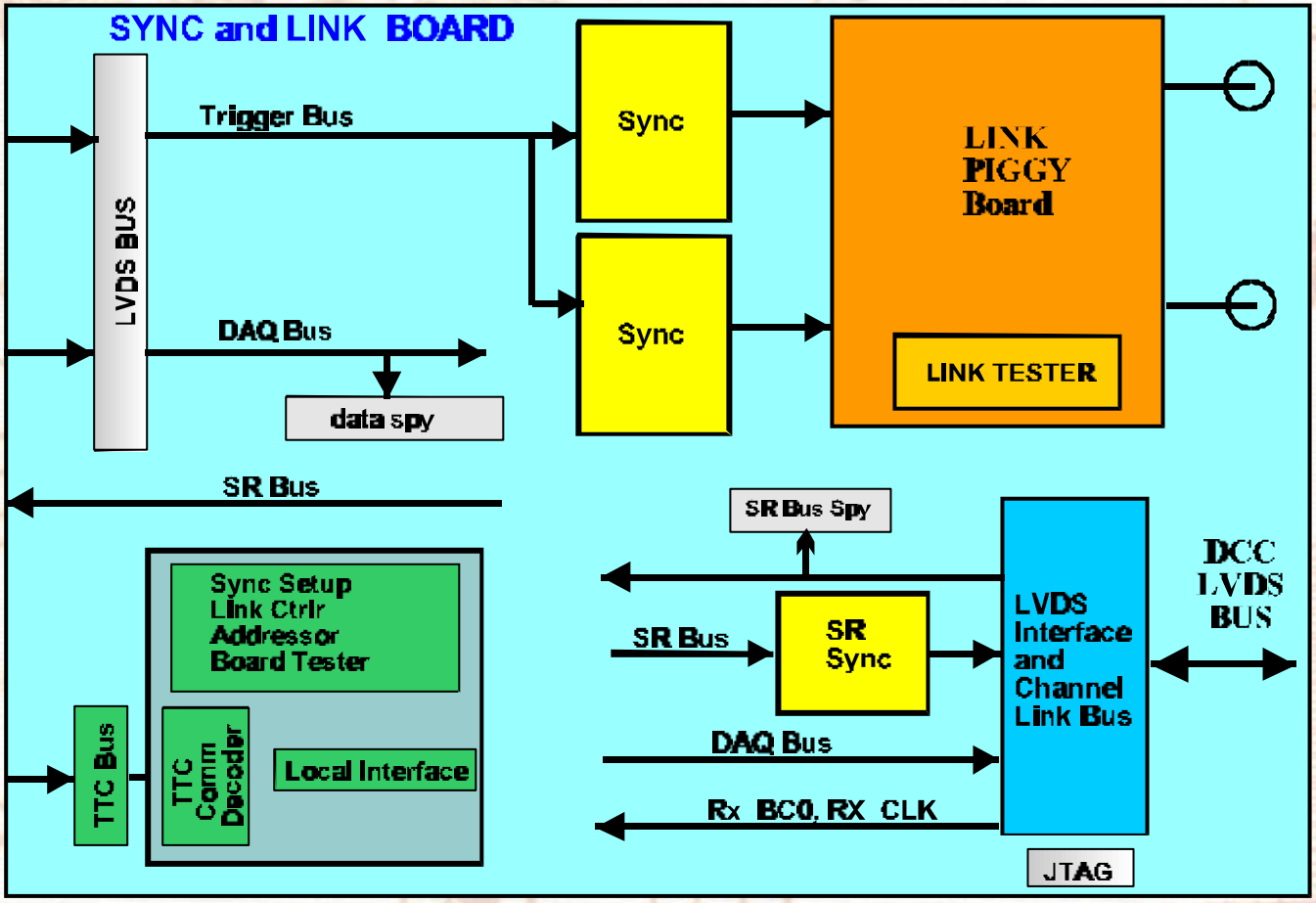
SLB, Synchronization and Link Board

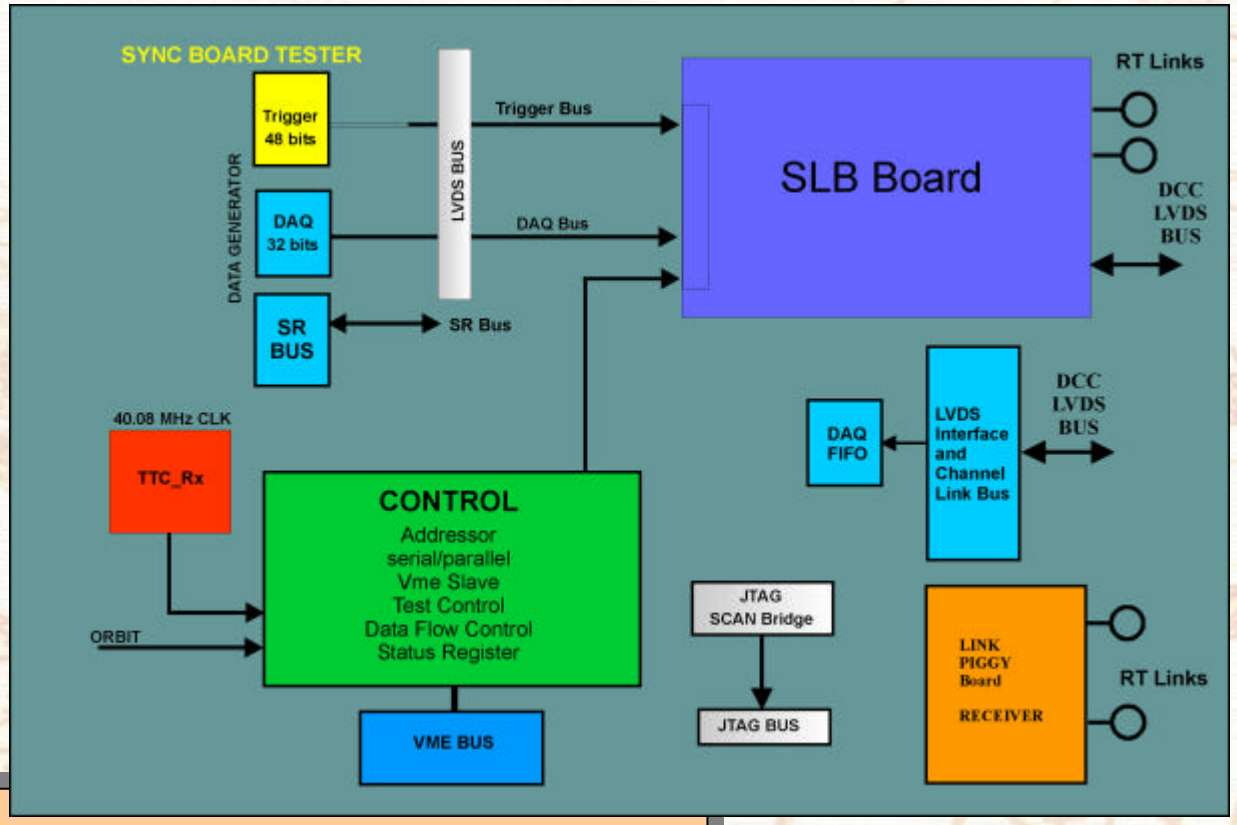
Trigger Synchronization Test Setup in 97



SLB, Block Diagram

ULRT board interface

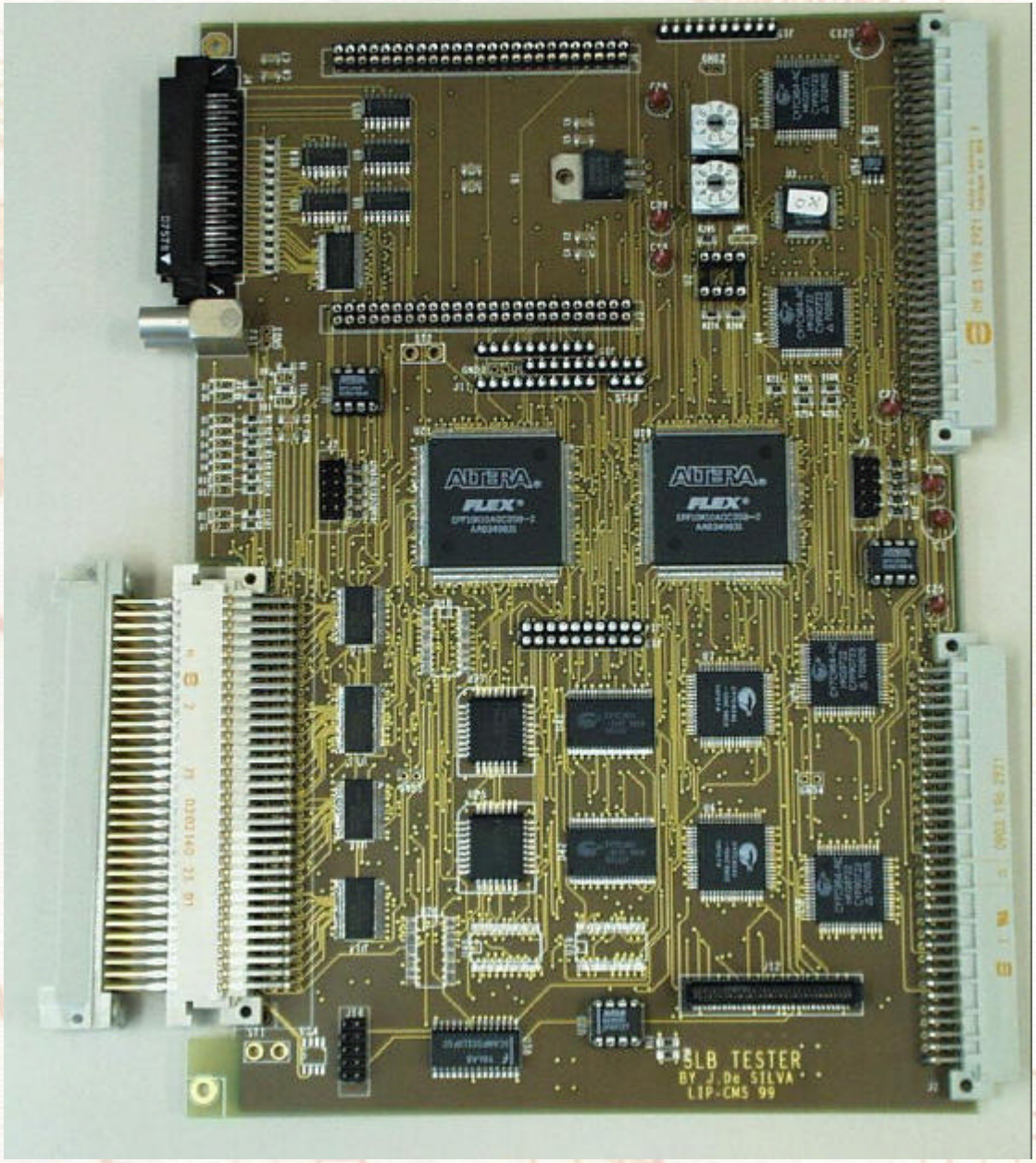




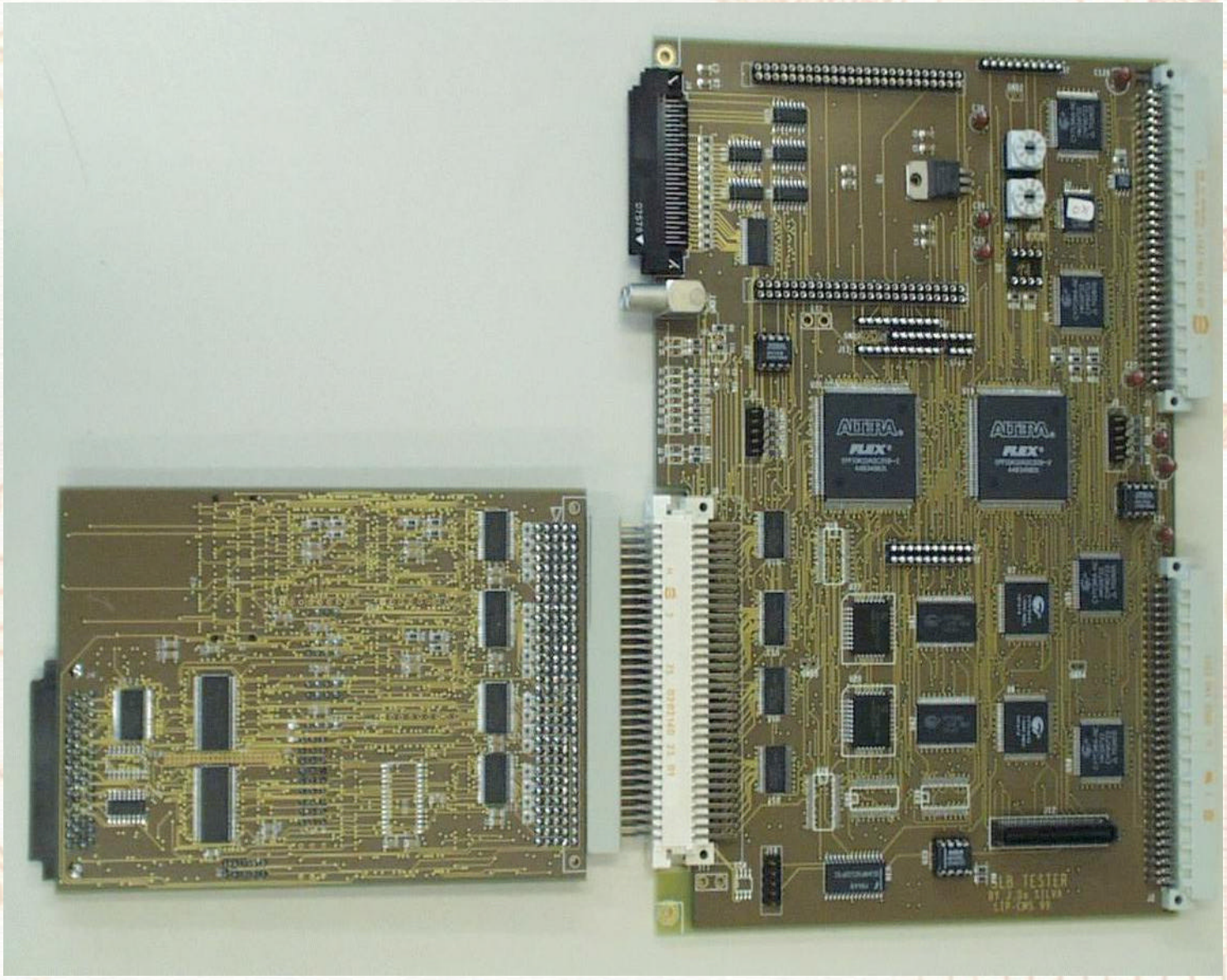
SLB TESTER,
Block Diagram

- **Trigger Path generation (2TT)**
- **DAQ Data Burst Stream Gen**
- **SR Controller implementation (DCC)**
- **ROSE 50 interface (Rose100 Design)**
- **DCC input port**
- **RT link receiver (piggy board)**
- **Embedded LHC structure**

SLB TESTER



SLB TESTER - SLB



SYNC 2K

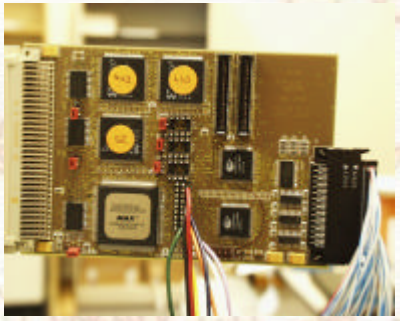
- **New Version of the SYNC circuit (LIP)**

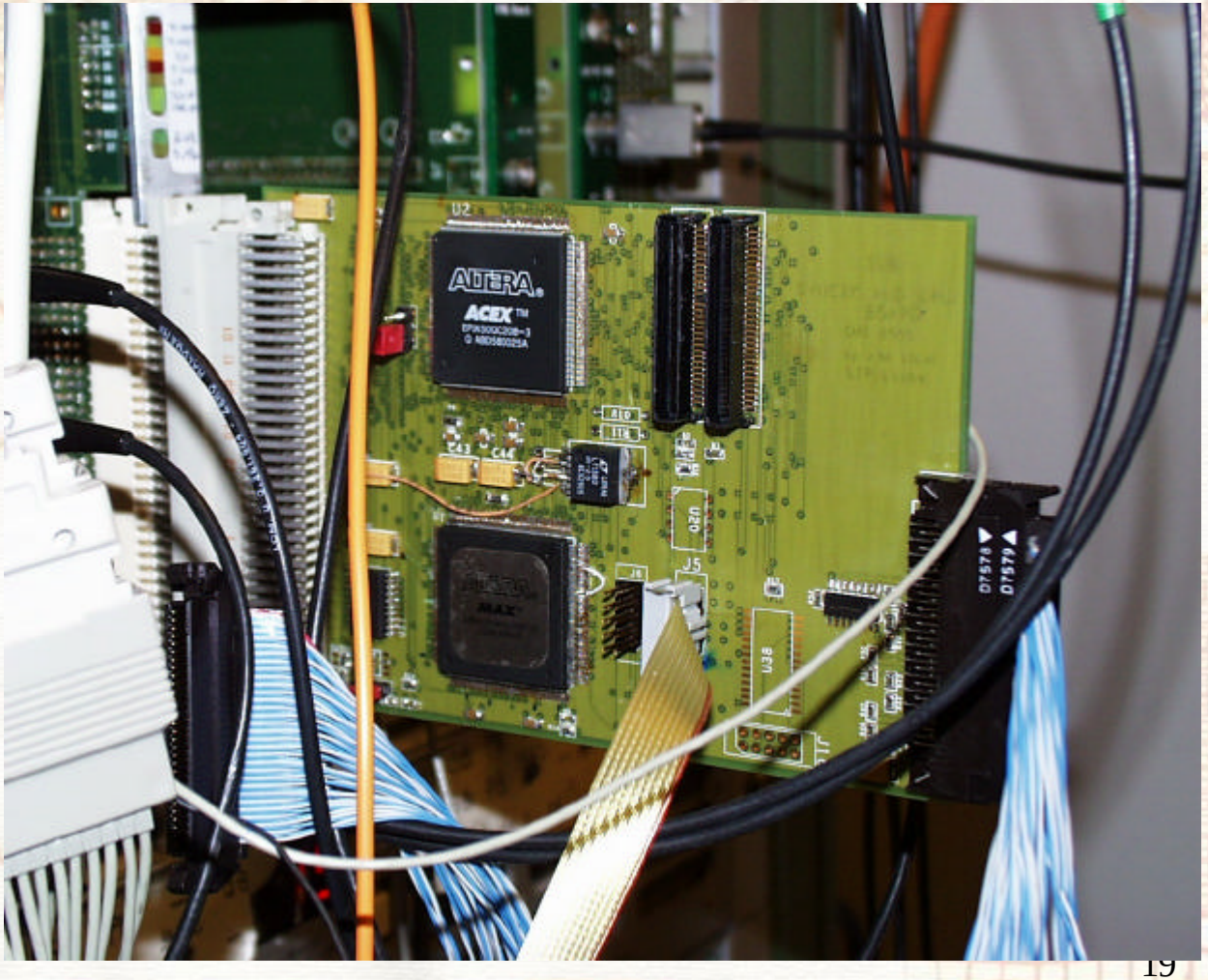
(Design started in September, under test)

- **2 in 1 (ALTERA 1K)**
- **Accumulator of 1024 bunch xings**
- **1 Clock latency (minimum)**
- **BIST (to be implemented)**

SLB-SYNC 2K

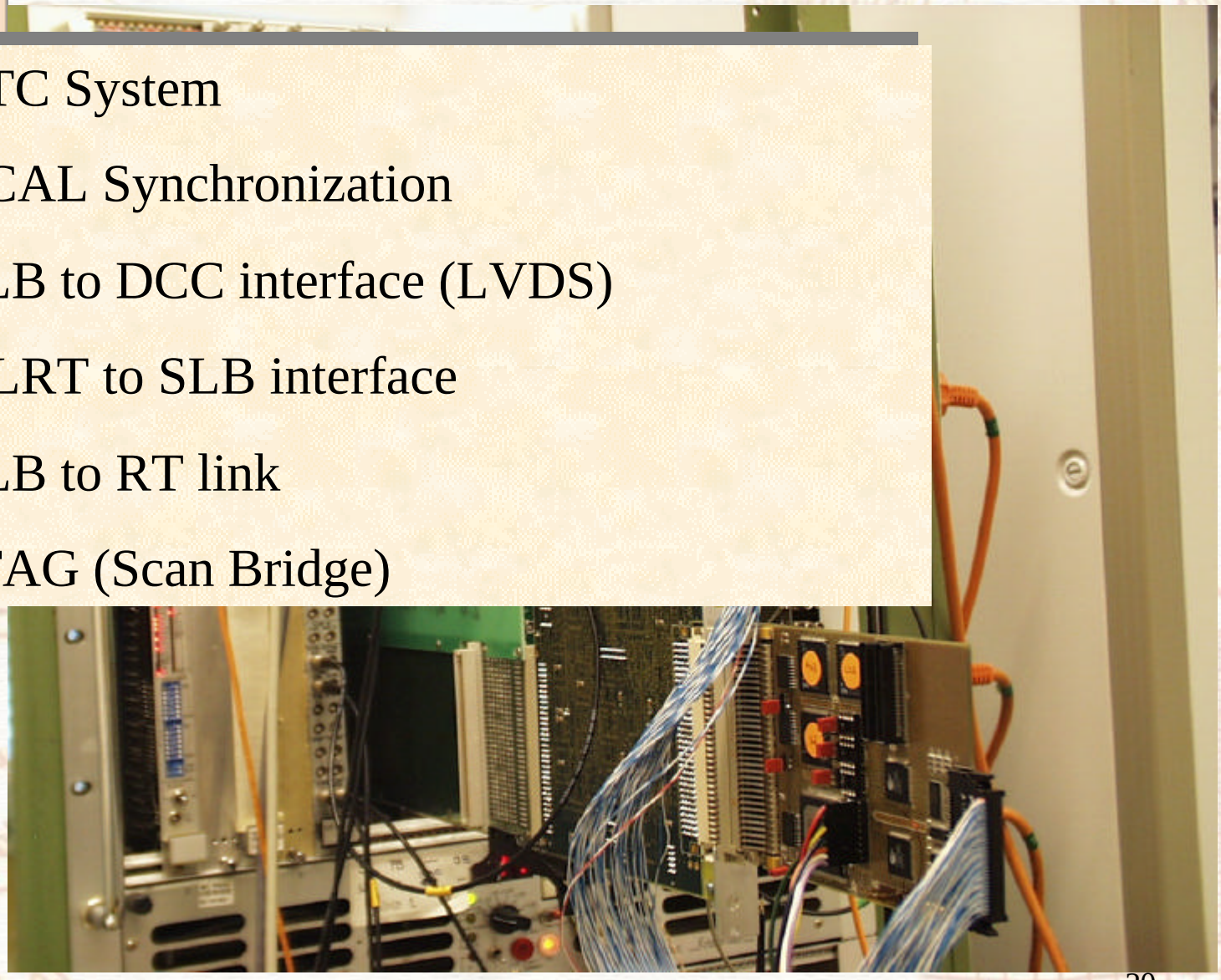
- **New Version of the SYNC circuit (LIP)**





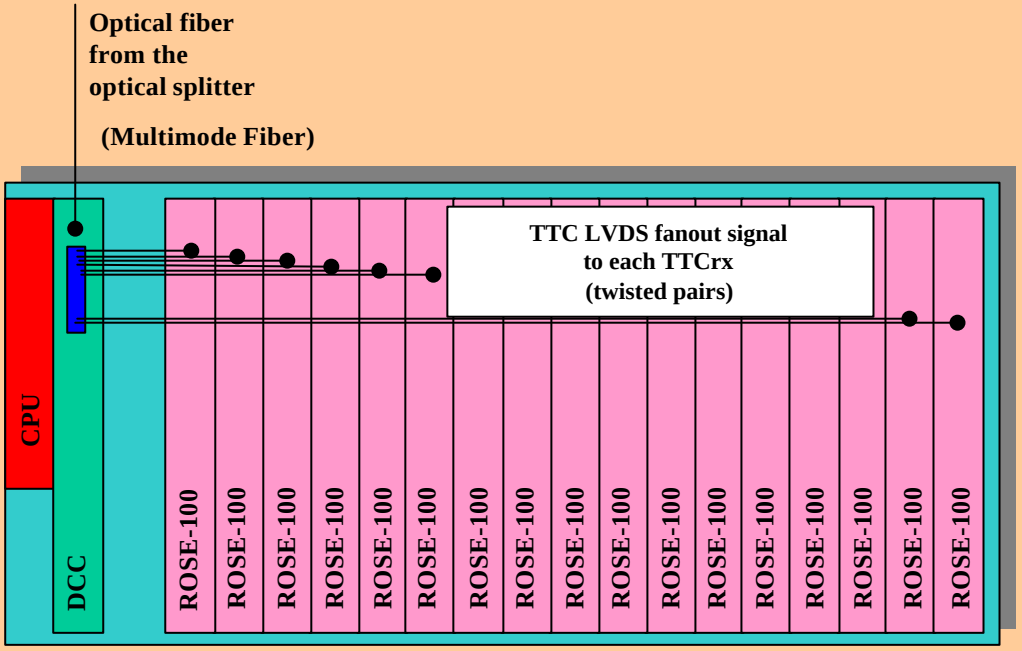
1999-2000 Test Bench

- TTC System
- ECAL Synchronization
- SLB to DCC interface (LVDS)
- ULRT to SLB interface
- SLB to RT link
- JTAG (Scan Bridge)

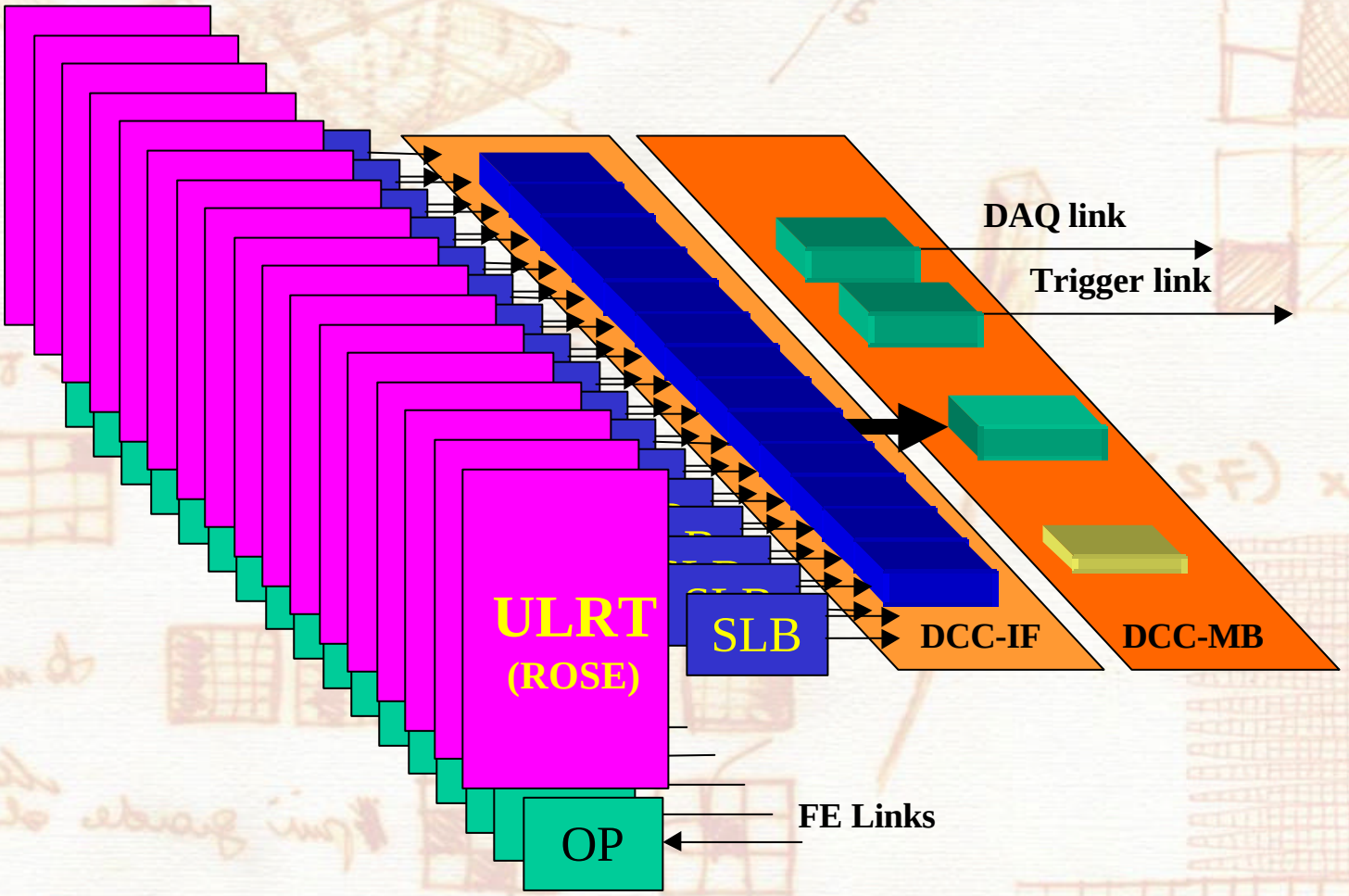


DCC,
ECAL Data Concentrator

Example of an ECAL (Barrel) 9U Crate



ECAL Crate Overview



DCC Partition

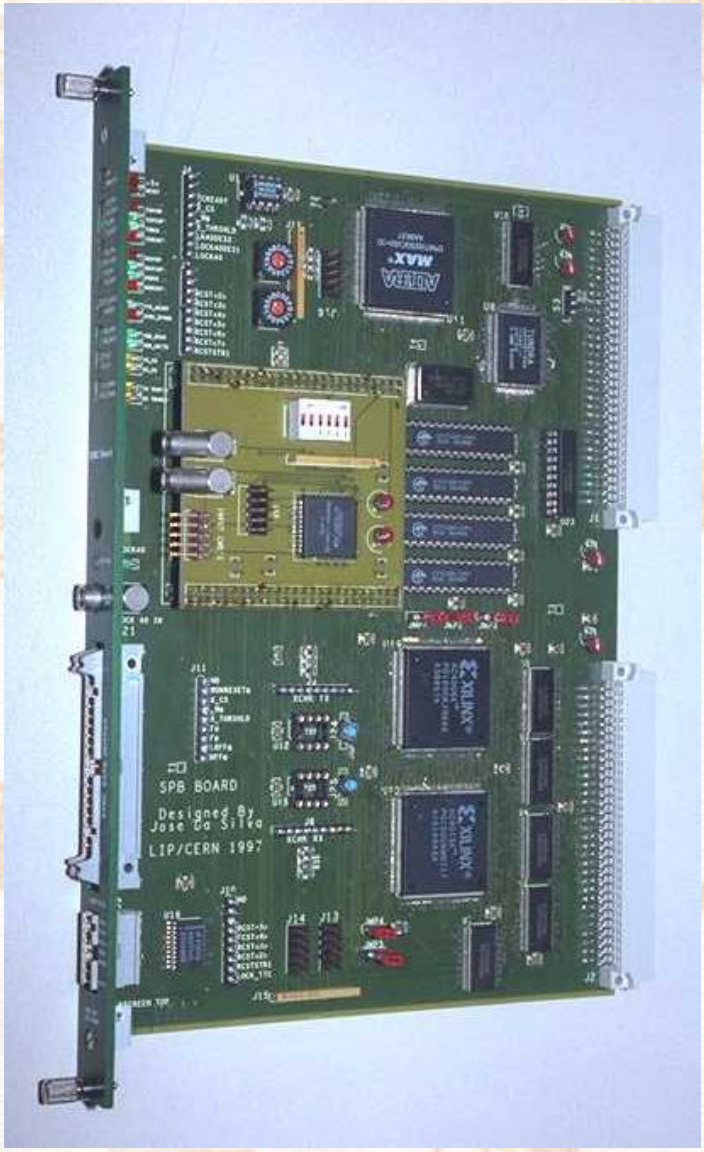
- **DCC-MB (9U)**
  - Event Builder
  - DAQ link
  - Trigger link
  - CPU-Link
  - TTC fan-out
  - MB of the DCC-IF

- **DCC- IF (6U TB)**
  - 17 channels
  - SR processor implementation

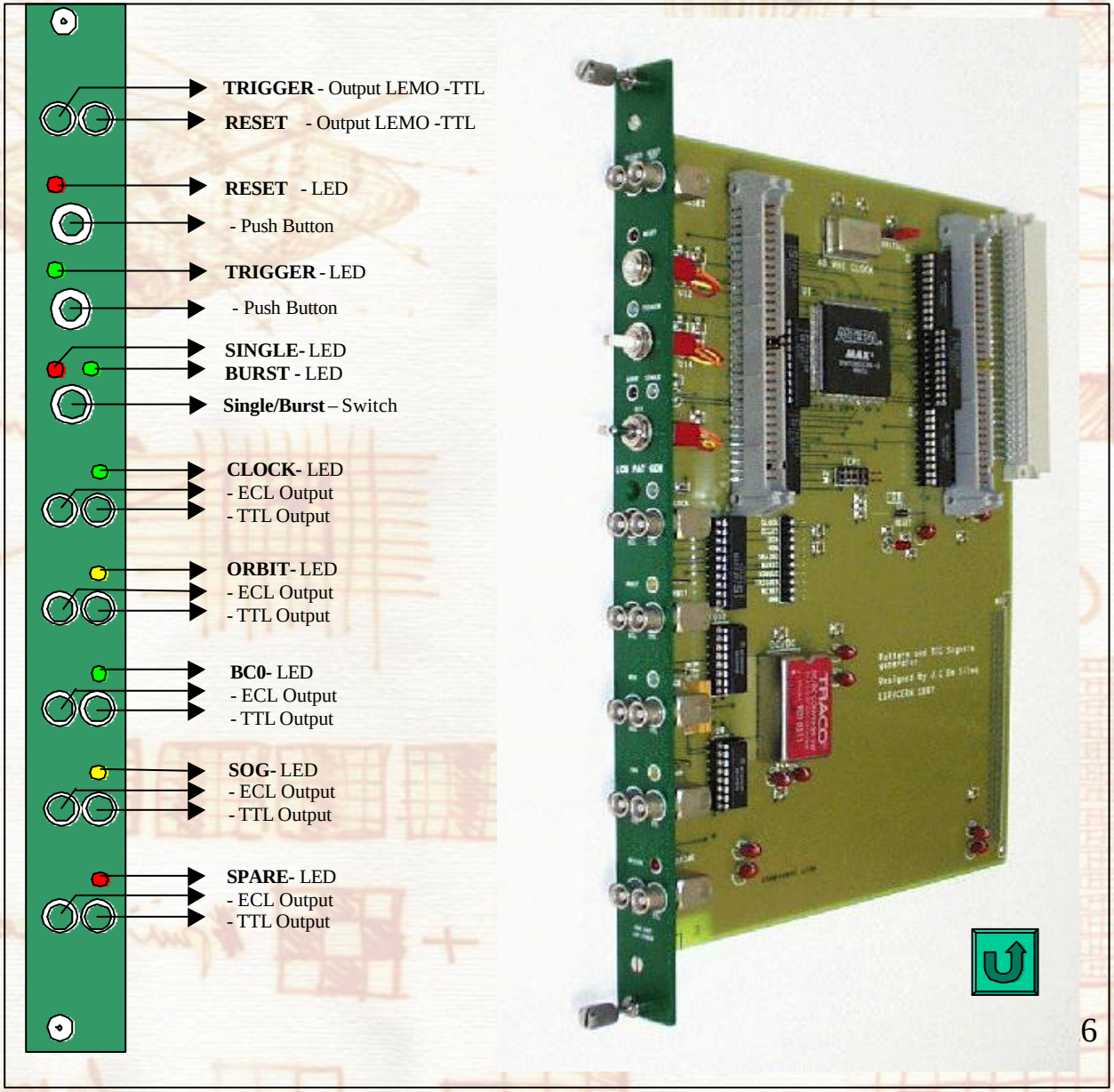
Future work

- **SYNC2K**
  - Quality tests and BIST
- **DCC**
  - design and tests - proto June 2001
- **RT link tests**
  - Summer 2001
- **TCC**
  - end of the year

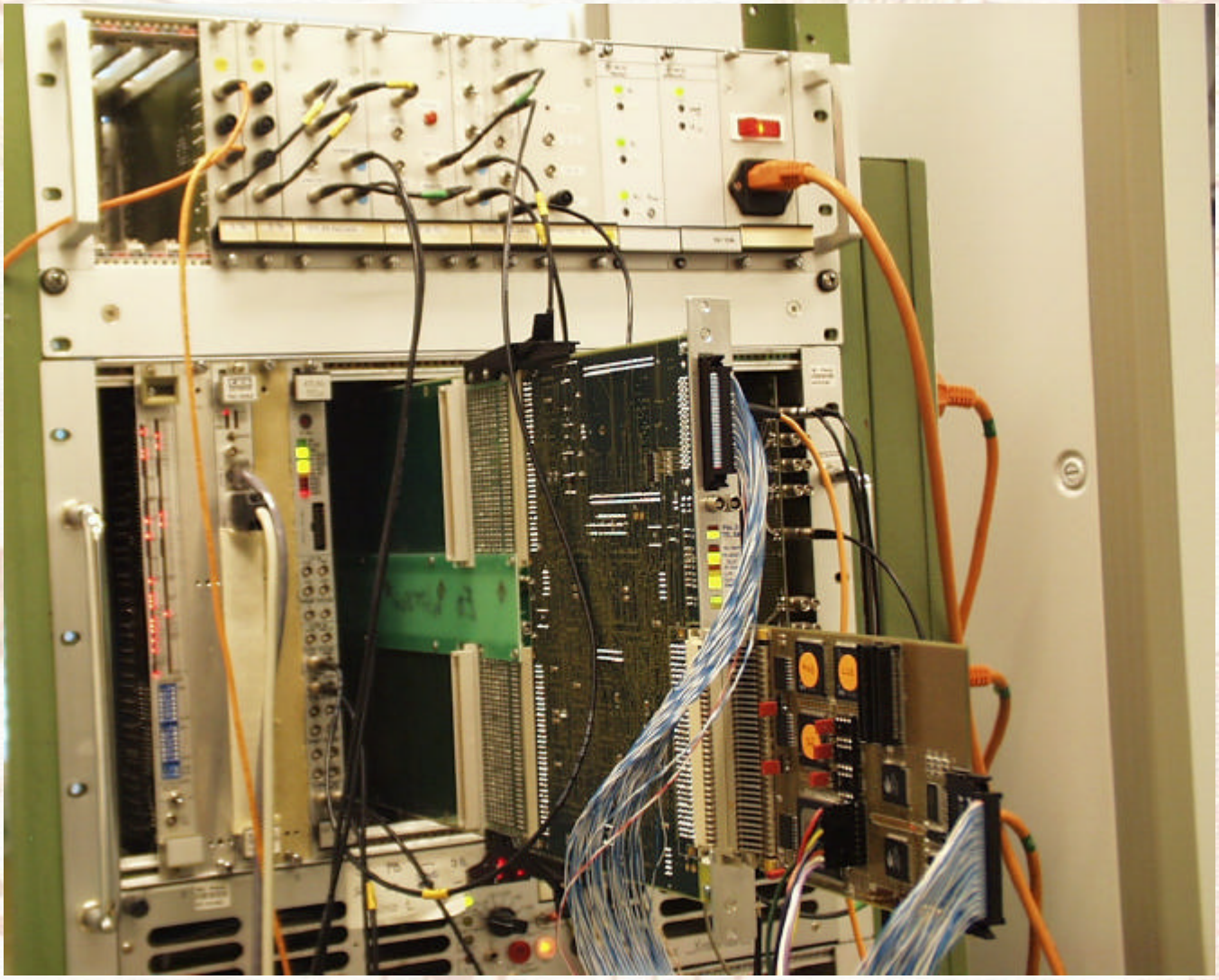
SPB,
Sync TX and Sync RX



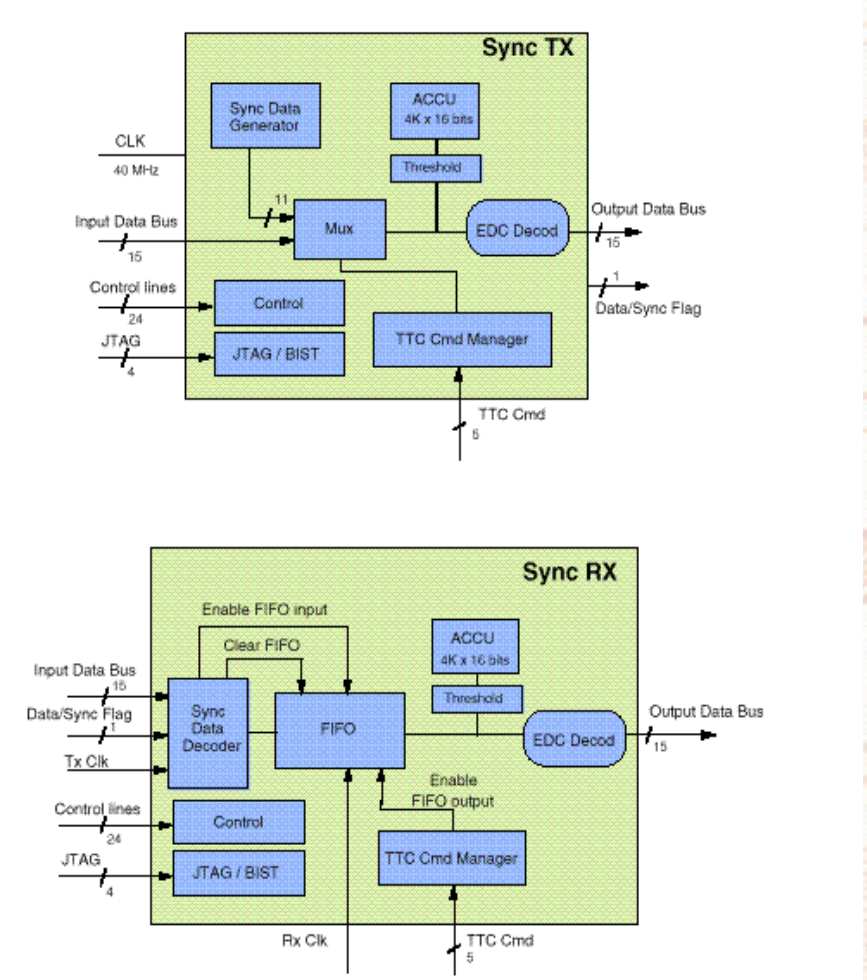
LHC Generator



TTC System



SYNC TX and SYNC RX



- **2 circuits implementation with external RAM to perform accumulator functions**

ECAL TTC tree