Chapter 1

Design and implementation of an autonomous DAQ system

The need to have a simple, low-cost, stand-alone data acquisition system for cosmic ray experiments led to the development of the LIP-PAD board. The DAQ system of ULTRA and TRC were implemented using such boards. A new generation of LIP-PAD, named LPV3, is being developed in order to increase the acquisition performance and its autonomy. The LPV3 will have the capability to control external hardware, to acquire data by itself and communicate the data through network protocols.

1.1 LIP-PAD board

The LIP-PAD board was developed at LIP as a joint effort between the groups working on the ULTRA experiment and on the TRC project. The two main features characterising this board are:

    - sampling, synchronously, analog signals coming from PMTs;

    - time tagging the acquired data using an external synchronisation pulse (e.g. the pulse from a GPS unit).

    The board communicates with a PC through the PCI protocol. A brief description of the board and its application in the ULTRA experiment are given in the next sections. A more detailed description of the board and its functionalities was presented elsewhere [3].

1.1.1 Board Description

The LIP-PAD board, shown in figure 1.1, has two main functional blocks: The Analog Acquisition Sub-system (AAS) and the Time Measuring Sub-system (TMS). The main component of the board is a FPGA where most of the digital electronic components are implemented.

    The AAS performs the digitisation of analog signals from PMTs. It is composed of six channels, each having a shaper followed by a 10 bit ADC running at 100 MHz. The shaper stretches the PMT signal and inverts its polarity as required by the
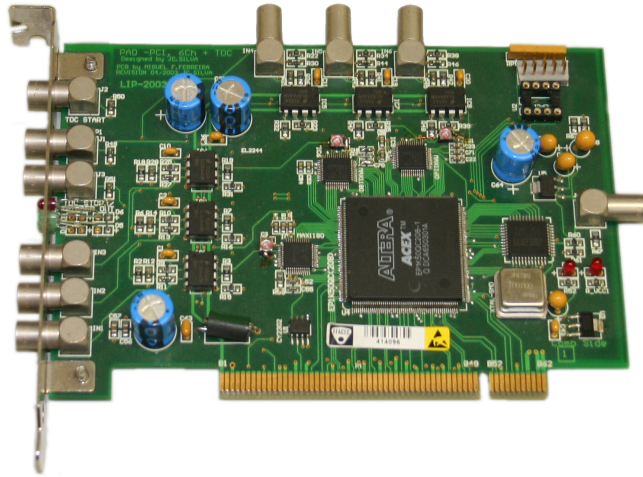
Figure 1.1: The LIP-PAD board (version 2).

ADC input. The outputs of the ADCs are directly connected to the FPGA. These signals are routed internally to the trigger unit and to a buffer memory. A fraction of a FIFO memory, that is constantly written and read, is used used to buffer the data. When the triggering condition is met the FIFO memory is filled. In this way the data acquired will have a pre-trigger and a post-trigger component.

The TMS measures the time between the trigger signal (internal or external) to an external synchronisation pulse. If this pulse is synchronised to the UTC (as is the case when GPS signals are used) it is possible to time-tag the trigger signal using the UTC time. The time measurement is done using a counter and a clock running at 50 MHz, implemented in the FPGA, and a TDC controlled by the FPGA.

The board has a control unit, responsible for the management of data and operation, and a PCI client, responsible for the interface with the host computer. The board is designed so that the FPGA can be programmed by a PROM that will load its contents to the FPGA when the host PC boots. However the board can also be programmed using a cable connected to an external PC, making the board extremely flexible since it can be easily reprogrammed.

1.1.2 Performance in the ULTRA experiment

The LIP-PAD board was the main block of the DAQ system used for the successful run of the ULTRA experiment at Capo Granitola, Sicily, Italy. The run setup is described in section **??** and also in [2].

DAQ configuration

The DAQ system was designed to acquire data from different types of detectors used in the experiment. The signals can be grouped in four different classes: high gain ETScope PMT signals, low gain ETScope PMT signals, UVScope PMT signals and Belenos PMT signals.
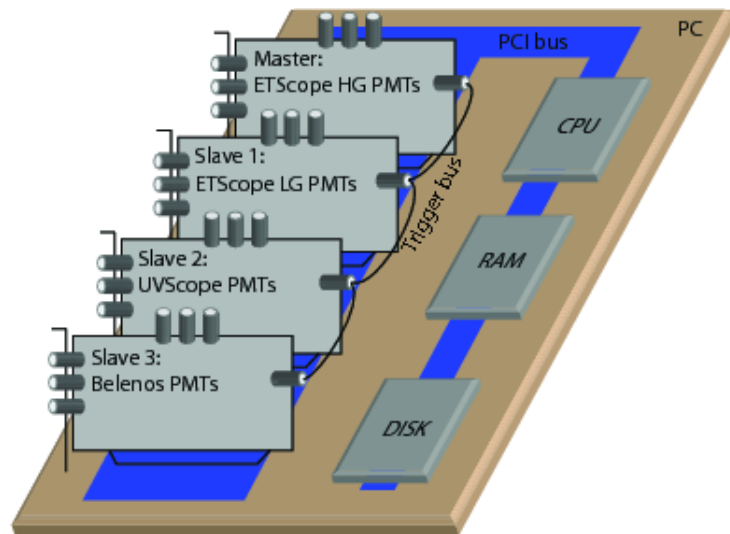
Figure 1.2: Scheme of the ULTRA data acquisition setup. The ULTRA DAQ consists of a PC with four LIP-PADs working in Master-Slave mode

Each station of the ETScope is equipped with two PMTs that are operated with different gain settings thus extending the dynamic range of the station. The High-Gain PMTs can record the signal from low multiplicity events (down to a m.i.p. signal) while the Low Gain PMTs are able to collect high multiplicity events that saturate the High-Gain PMTs. The gain settings of the PMTs guarantee that the two dynamic ranges overlap, allowing inter-calibration of both PMTs. The lower threshold and faster response of the High-Gain PMTs makes them suitable to be used for triggering and for the estimation of the primary cosmic ray direction which is based on time differences. The synchronisation between the High-Gain PMT signals is thus crucial. The signals from the UV scope are used to measure the UV light reaching the detectors, scattered from the water. The Belenos detectors are UV detectors placed in the centre of the array to collect directly the UV light arriving with the EAS.

Figure 1.2 shows a scheme of the ULTRA DAQ system. In figure 1.3 photographs of the system on-site are shown. The DAQ system consists of four LIP-PAD boards configured in a Master - Slave scheme installed in one PC. The signals from the ETScope PMTs with high gain are connected to one board that acts like the master board. These five signals, connected to the same acquisition board, are acquired synchronously. Since all the channels on the board are sampled using the same 100 MHz clock, time differences between them have a precision of 10 ns. The signals from the ETScope PMTs with low gain are connected to the board slave #1. Slave #2 acquires signals from the two PMTs of UVScope while slave #3 acquires data from the Belenos PMTs. The master board defines a trigger using the information from all the five signals of the high gain ETScope PMTs and sends the trigger signal to the slave boards through a trigger bus. Each slave board receive this signal that act as an external trigger to the board. Although the acquisition is not synchronous between the boards, the data are acquired simultaneously within a latency of few

Figure 1.3: Photographs of the ULTRA DAQ at Capo Granitola. Left: Global view of the system. Signal cables arrive from the left and are connected directly to the LIP-PADs. Right: Detail of the four LIP-PADS installed in the acquisition PC.

tens of ns. This time latency is sufficient to ensure that the data recorded by all detectors belong to the same event.

Trigger system

The Trigger system implemented in the master board FPGA has two levels. The first trigger level consists of a digital threshold applied to the data acquired by each ADC. The threshold for each channel is defined independently from each other. The threshold chosen must take into account the baseline value and the noise of the corresponding channel. The second level trigger is an online logic trigger that can work, basically, in two modes: single event mode and shower mode. In the single event mode a first level trigger from any of the active channels causes the system to issue a trigger signal. In the shower mode coincidences between stations are searched. A first level trigger in a channel opens a time window defined by the user. During this time window each first level trigger signal sets a latch. At the end of the window the number of positive latch outputs give the number of channels with signal above the threshold value during the time window. This number is compared with the required number of coincidences and a second level trigger is issued if the condition is met. At the end of this process the latches are reset.

DAQ software

The DAQ software was implemented in LabView using a PCI driver developed at CERN [4]. The LabView GUI communicates with the LIP-PADs by reading and writing its registers mapped to the PCI memory space. Figure 1.4 illustrates the main screen of the GUI. The GUI allows the user to select the board to be used as master and the boards to be used as slaves, the threshold levels, the trigger parameters, the file to store data and the number of events to be acquired. When the user starts an acquisition all the boards are programmed with the parameters chosen prior to the start of the acquisition. When the acquisition starts the GUI starts a process of polling to check if the master board has triggered. In this case

Figure 1.4: View of the GUI of the acquisition program from the Capo Granitola setup. In the figure it is shown the acquisition control menu of the GUI

all the four boards are read and then reset. During the acquisition the user has the possibility to view, in a graphic window, the data acquired by the system. Acquired data is saved in a binary file for offline analysis.

Signal reconstruction

The signal time and charge collected are estimated from the data acquired by the LIP-PAD which consists on a set of signal voltage samples taken in 10 ns intervals. The signal time and collected charge can be estimated directly from the data as, respectively, the time corresponding to the first sample that is above the threshold and the sum of all samples. A more sophisticated approach involves fitting an empirical parametrisation to the data and use the fit result to estimate the signal parameters. The data can be described by an empirical parametrisation of the form

$$V\left(t\right) = C \cdot e^{-\frac{1}{2}\omega^2 \log^2\left(\frac{t-t_0}{\Delta}\right)}$$

where C is the peak amplitude, ω is a shape factor, t_0 is the initial time of the signal and Δ is the rise time of the signal. This formula is fitted to the data leaving these parameters free. A first estimation of t_0 and C is done recurring to the time of the first sample above a threshold and the maximum value recorded, respectively. The parameters ω and Δ are initialized to constant values. The signal time is evaluated using a constant fraction discrimination set at 20%. The time is then given as

$$t_{20\%} = t_0 + \Delta \cdot e^{-\left(2\omega^2 \cdot \log(5)\right)^{1/2}}$$

The collected charge is proportional to the integral of the signal and can be evaluated as

$$Q \propto \int V\left(t\right) = C \cdot \Delta \cdot \omega \cdot e^{0.5\omega^2}\sqrt{2\pi}$$

A sample pulse acquired by the LIP-PAD is represented in Figure 1.5. The plot represents the signal amplitude in ADC units versus the time in 10 ns units. The baseline of the channel has been subtracted from the data. The solid line represent the fit result to the empirical formula.
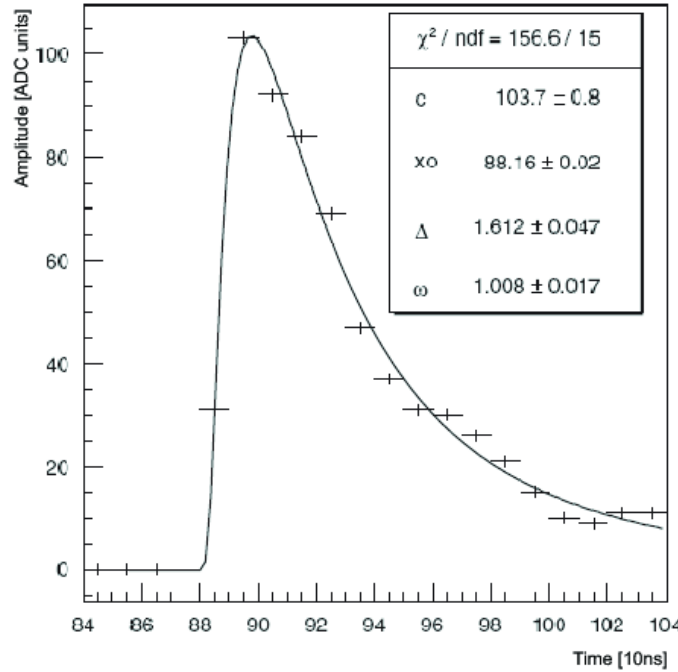
Figure 1.5: A sample pulse from one DAQ channel is showed. The plot represents the signal amplitude in ADC units versus the time in 10 ns units. A fit is superimposed to the data. See text for details.

Calibration

The calibration of each scintillator was performed by measuring the Vertical Equivalent Muon (VEM) signal of each scintillator. First, the high voltage power supply of the low gain photomultipliers was raised so that the two PMTs of each station have the same gain. Data acquired in this mode is represented in figure 1.6 where the integral of each recorded pulse for PMT2 of station 1 is plotted against the value for the PMT1 of the same station. The distribution of the collected charge in single acquisition mode for both PMTs of station 1 is shown in figure 1.7 where the pedestal peak in the lower part of the spectrum followed by the single particle spectra is clearly seen. The pedestal, due to uncorrelated noise, was suppressed imposing a coincidence trigger between the two PMTs as shown in figure 1.8. The value of the integrated pulse corresponding to the most probable value for the deposited charge in a PMT, when a single particle crosses the scintillator, was taken as the VEM calibration constant. This constant allows the collected charge to be converted to the equivalent number of particles crossing the detector.

Data runs

The data run lasted for seven months from spring to winter 2005. The setup worked for ~ 309 h and a total of 5682 events were acquired. From these 216 have signal both in the ETScope and in the UVScope. The data analysis of the collected data is described in [5]. An example of a "golden" event is shown in figure 1.9. Each graph
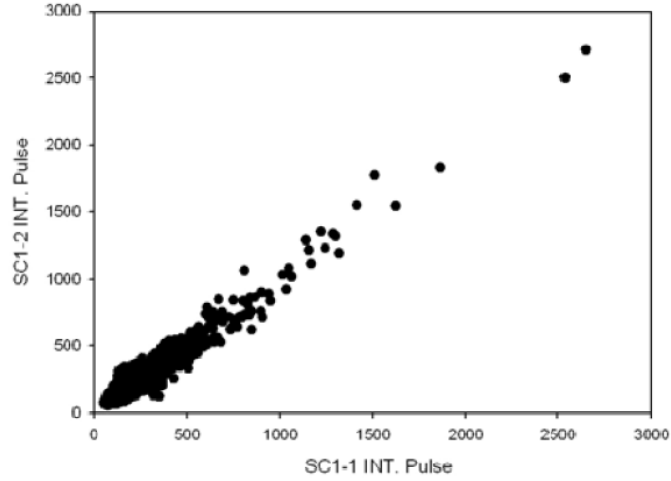
Figure 1.6: Plot of the integral of recorded pulses for PMT2 versus PMT1 in ADC
units. The HV was adjusted so that the gain of both PMTs is the same.

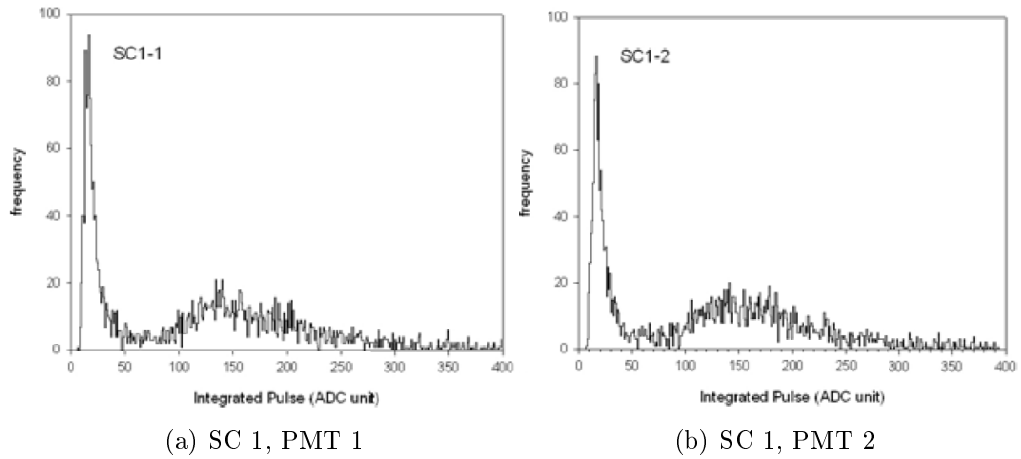(a) SC 1, PMT 1   (b) SC 1, PMT 2

Figure 1.7: Distribution of the integral of acquired pulses in single acquisition mode
for both PMTs of station 1. The gain of the PMTs is set to be equal.

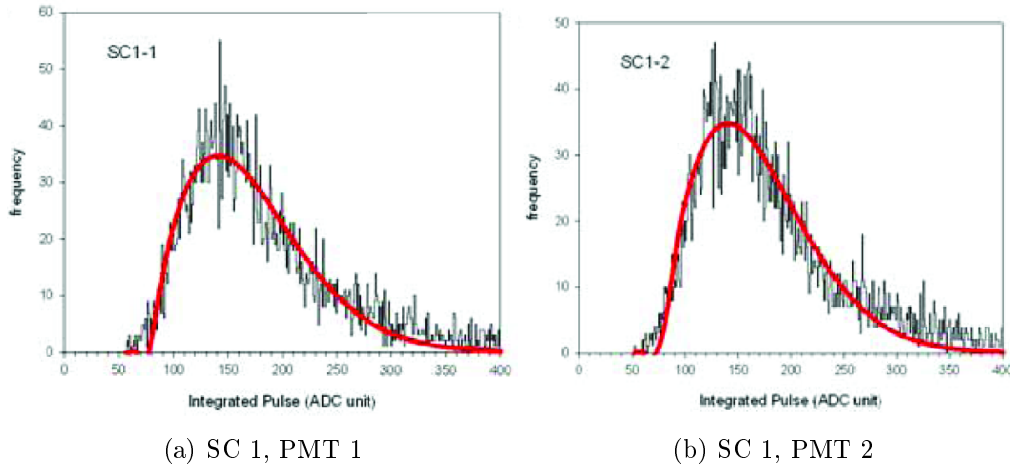(a) SC 1, PMT 1   (b) SC 1, PMT 2

Figure 1.8: Distribution of the integral of acquired pulses in coincidence acquisition mode for both PMTs of station 1. The gain of the PMTs is set to be equal.
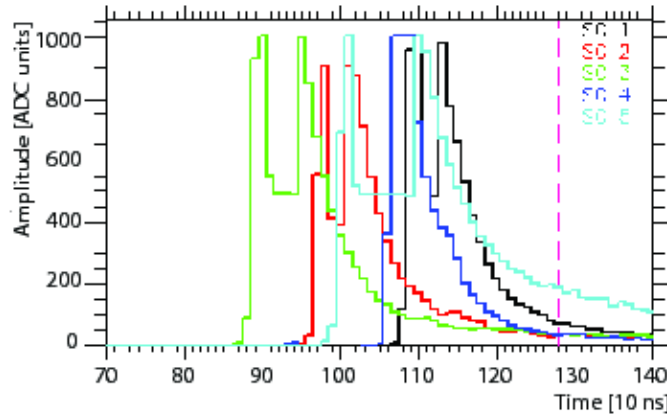
shows the signal amplitude recorded by the DAQ system, in ADC units, versus the time in 10 ns units. The top graph shows the signal for High Gain PMTs where the saturation of most PMTs is visible. The middle graph shows the Low Gain PMTs signals where no saturation is visible. The bottom graph shows the data collected for the UVScope and Belenos. In every graph the expected time of arrival of the light at the UVScope is marked with a vertical dashed line. It can be seen, in the bottom graph, the good agreement of the collected signal by UVScope with the expected time of arrival.

In previous runs of the experiment a similar system based on LIP-Pads has been tested in comparison with a traditional one based on CAMAC and NIM [3] reproducing the results from the CAMAC system with the benefit of lesser saturation. The experiment gained also the sampling of the signals in time which was not possible with the NIM-CAMAC system. This feature was essential to discriminate particle and diffused Cherenkov light signals in the UVScope. The system proved to be efficient and reliable contributing decisively to the success of the experiment.

1.1.3 Application in the TRC

The Lisbon Cosmic Ray Telescope (TRC) [6] is an outreach project of cosmic ray physics aimed at high school students. The project consists of a network of cosmic ray detectors installed in high schools. Each high school counts with an autonomous detector of cosmic rays composed by three scintillator detectors, usually installed at the roof. The separation between the scintillators is constrained by the space available at the rooftop and is usually of few tens of metres. The network counts also with a central station installed at Instituto Superior Técnico (IST). The distance between the different 9 stations installed at Lisbon ranges from 2 to 10 km. Two other stations are installed in the city of Beja at a distance of ~ 137 km from the central station at IST. The stations can also operate in coincidence mode. In such mode data is acquired simultaneously with a predefined setup and the data can be
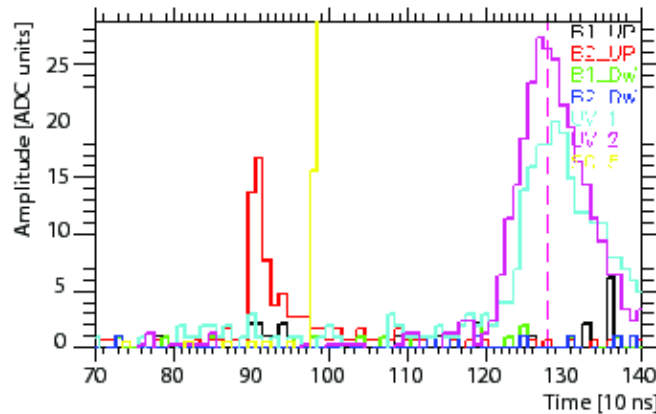
(a) High Gain ETScope PMTS
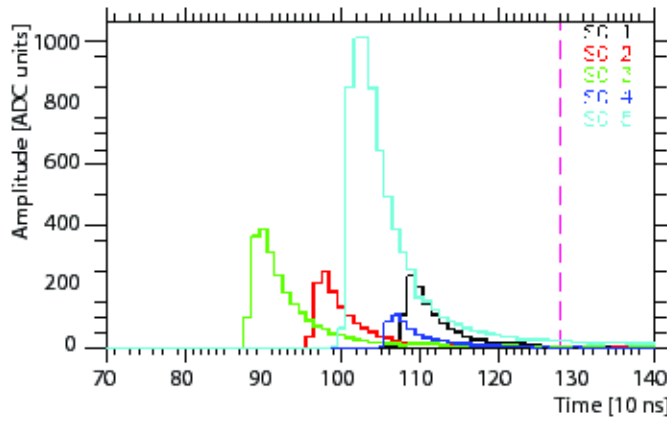
(b) Low Gain ETScope PMTs

(c) Belenos and UVScope PMTS

Figure 1.9: A sample event recorded by the LIP-PADs. Each graph shows the signal
amplitude in ADC units versus the time in 10ns units. (a) shows the signals recorded
from the High Gain ETScope PMTs; (b) shows the signals from Low Gain ETScope
Photomultipliers; (c) shows the signals from Belenos and UVScope Photomultipliers.
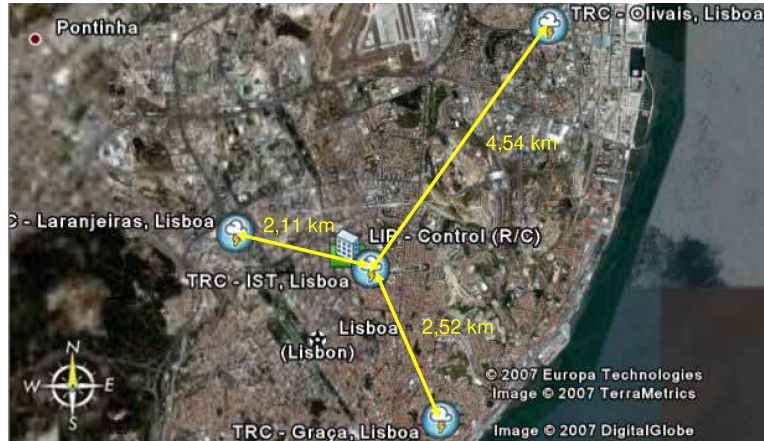
Figure 1.10: Map of the three schools and the central station at IST that participated in the run in coincidence.

joined. Using the recorded time for each event coincidences in data can be searched. Recently a test run in coincidence mode was performed with three schools and the central station at IST. A map with the participating stations is presented in figure 1.10 .

Each TRC station has a DAQ and control system, illustrated in figure 1.11, that consists of a LIP-PAD installed in a PC. The system controls the HV power supplies through an I2C link. The I2C protocol is emulated using the parallel port of the acquisition PC. The GPS communicates with the PC by an RS232 link connected to the serial port. The PPS signal from the receiver is connected directly to a digital input of LIP-PAD. Each PMT signal is connected to an analog input of the LIP-PAD.

The detector is usually placed in the roof-top of the school while the DAQ system is placed in a room with restricted access. Thus, the detectors have a large separation from the DAQ and control system. The cabling of one TRC station comprises 3 signal cables, one for each PMT, a PPS cable, a RS232 cable, an I2C cable and one for 12 V power supply. The distances involved in cabling are quite large, of the order of 100 m.

The main problems that arose in the TRC DAQ and control system are related with the time-tagging and the operation system stability and robustness. The problems in time-tagging derive from the performance of the DAQ PC that manages the TMS and the GPS. The time-tagging system requires that the time information stored in the LIP-PAD is combined with the GPS information received by RS232. The PC must also read and reset the timing registers of the board. Due to the high load of the DAQ polling process some times these operations are not performed within the necessary time causing the time-tagging system to fail.

Operation stability and system robustness of the TRC needs to be improved. Problems in the DAQ PC are common. Problems in cabling are also an issue to be addressed. The long distances involved complicate the system debugging, namely for cable testing
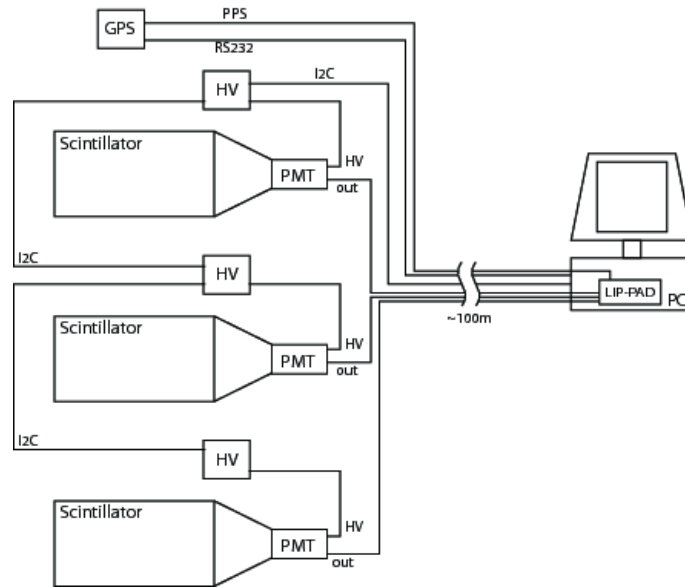
Figure 1.11: Scheme of the DAQ and control system installed in each station of the TRC project.

1.2 LPV3 (Lip-Pad Version 3)

A new DAQ board is being developed. This board is designed to be a complete DAQ and control system, thus eliminating the need for a DAQ PC, for small cosmic ray experiments that use up to six photomultipliers. Although inspired by the LIP-PAD board it is designed from scratch since all the elements have changed and some were added. This is reflected in the name LPV3 that derives from the acronym - LIP-PAD version 3.

1.2.1 Requirements

The LPV3 has evolved from the LIP-PAD board. LPV3 is intended to improve the performance of the LIP-PAD. Namely it has to meet two main requirements: operate in an autonomous way and improve the signal reconstruction with respect to the previous version. It is also expected that the new design will increase the maximum acquisition rate of DAQ systems based in the LPV3.

LPV3 is designed so that it can operate without being installed in a PC. In this case the control and read-out are performed using a network connection. In order to be a full DAQ and control system, the LPV3 must also control other hardware devices. Typically, cosmic rays experiments use PMTs, high voltage power supplies, GPS systems for synchronisation and weather stations that need to be interfaced by the LPV3. For this purpose standard protocols will be implemented (RS232, I2C). A general purpose Input - Output bank is foreseen so that other protocols can be implemented.

The communication through network and the ability to control other hardware implies that the LPV3 has processing capability and storage. This will be accom-
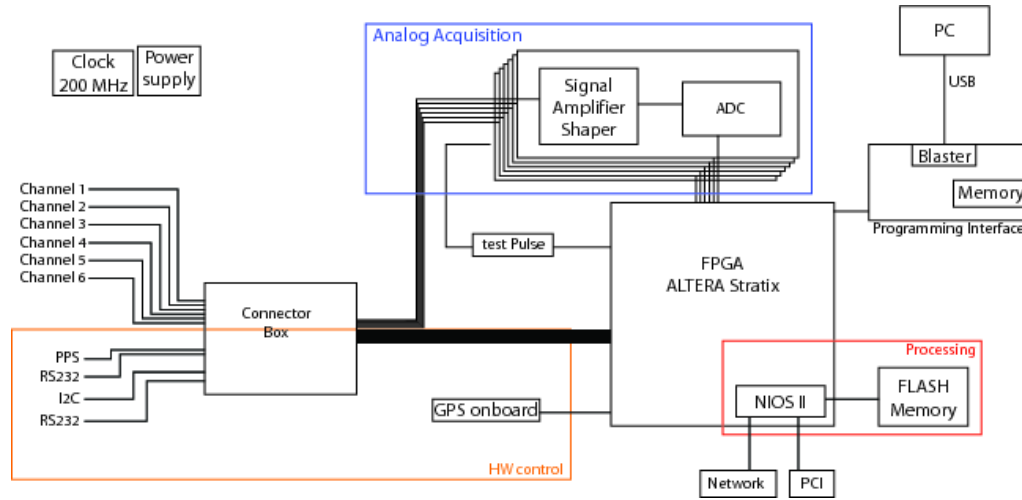
Figure 1.12: LPV3 block diagram

plished with the use of an embedded processor in the FPGA and an external memory.

The second main objective is to improve the estimation of each signal parameters: time and collected charge. This issue is addressed in two ways: (i) the sampling frequency and resolution of the ADC will be increased in LPV3 and (ii) the analog input stage will be redesigned so that the output signal of this stage will have a predefined shape and duration in response to a fast PMT pulse. The shaping parameters result from a compromise between having enough samples for the fitting procedure and the loss in time accuracy.

1.2.2 Design Options

The new LPV3 board will be implemented following the design requirements expressed in the previous section. Figure 1.12 shows the block diagram of LPV3. The main blocks of LPV3 are: programming interface; processing; analog acquisition; hardware control; network interface; PCI interface. The implementation of these main blocks will be discussed in the following paragraphs. The core piece of the board will be the Altera Stratix FPGA[1] that provides sufficient resources to implement all the digital electronics of the board working at the required frequency.

Programming interface

The FPGA of the LPV3 will be able to be programmed using a cable connected to an external computer or by a memory. When the memory is used, the data contained in the memory will be transferred to the FPGA when the board is reset. The memory is non-volatile and can be reprogrammed using the external cable. This scheme will give total flexibility to the board. A stable configuration can be loaded in the memory, development firmware can be tested by reprogramming using a cable and the updates to the board firmware will then be performed by simply reprogramming the internal memory.

Processing

The imposed requirements forces the board to have processing capability. This will
be achieved by implementing a NIOS processor in the FPGA. The board must be
able to run acquisition software and to store the acquired data before sending it
through network. A flash memory will be installed to store both the acquisition
program and the acquired data. Flash memory was chosen because it is non-volatile
and thus the acquisition program will be saved even without power.

Analog acquisition

The analog acquisition block is an essential part of the system and it is the one with
more pressing requirements. As it can be seen from the block diagram (figure 1.12)
this block is composed by six analog acquisition channels. In each channel there is
an analog input stage followed by an ADC. The design of the analog input stage is
not finalised as some of the solutions need to be tested in hardware. A prototype
of LPV3 will be made with no signal conditioning stage. Instead the board will
have a connector with the input, output and power lines. The signal conditioning
stage will be then implemented in separate boards that will connect to the LPV3.
In this way the different solutions will be tested. It is still to decide if the signal
conditioning will be incorporated in the final version of the board or if the connector
will be maintained. In this case the boards can be customised with different shaping
and amplification circuits. However the connector might introduce more noise in
the analog channels than a standard solution and the final design requirements is
pending on the good performance in the prototype tests.

Hardware control

The board will be able to control several hardware. The LPV3 will have two RS232
connections, one I2C bus and an input line for the synchronisation signal. The GPS
unit will be controlled by RS232. Under study is the possibility to embed the GPS
in the LPV3 using a matching connector to the Motorola m12+ family of GPS. The
free pins of the FPGA will be used as general purpose I/O. These I/O lines will be
grouped in a generic connector. Several protocols can be implemented afterwards
in the firmware. A connector box will allow to interface the different connectors of
the protocols implemented.

Communications interface

The LPV3 will communicate both by PCI and by ethernet. The implementation of
the PCI will follow very closely the implementation of this protocol in the LIP-PAD
using the standard 32 pin 33 MHz PCI. The ethernet communication has already
been tested in development kits from Altera that include this protocol. In the kits
the NIOS and a driver for the implemented hardware was used. The hardware
implementation in the LPV3 will then be inspired in this design and will use the
same ethernet controller chip.

Abbreviations

AAS Analog Acquisition Sub-system

ADC Analog to Digital Converter

Belenos a detector of ULTRA

CAMAC Computer Automated Measurement And Control

CLF Central Laser Facility

DAQ Data Acquisition

ETScope Electromagnetic Telescope - a detector of ULTRA

FD Fluorescence Detector

FIFO First-In First-Out

FPGA Field Programmable Gate Array

GPS Global Positioning System

GUI Graphical User Interface

I2C Inter-Integrated Circuit (Serial communications protocol)

IST Instituto Superior Técnico

LIP Laboratório de Instrumentação e Física Experimental de Partículas, Portugal

LIP-PAD LIP - Placa de Aquisição de Dados (LIP - data acquisition board)

m.i.p. minimum ionizing particle

NIM Nuclear Instrumentation Module

PC Personal Computer

PCI Peripheral Component Interconnect

PMT Photo Multiplier Tube

PROM Programmable Read-Only Memory

RS232 Recommended Standard RS-232; A standard for serial binary data signals

SD Surface Detector

TDC Time to Digital Converter

TMS Time Measuring Sub-system

TRC Telescópio de Raios Cósmicos (Lisbon Cosmic Ray Telescope)

ULTRA UV Light Transmission and Reflection in Atmosphere

UTC Universal Time Coordinated

UVScope UV Telescope

Bibliography

[1] *Stratix II Device Handbook*, Altera Corporation, 2007.

[2] Agnetta, G., et al., Extensive air showers and diffused Cherenkov light detection: The ULTRA experiment, *Nucl. Instrum. Meth.*, *A570*, 22–35, 2007.

[3] Assis, P., The setup and engineering run of the ULTRA experiment, Master's thesis, Instituto Superior Técnico, 2003.

[4] Cano, E., Pci probe: simple labview vis for pci debugging, 2002.

[5] Catalano, O., and M. C. Maccarone, ULTRA experiment - report on the "Capo Granitola" campaign 2005, *Tech. Rep. 002/2005*, IASF-PA / INAF, 2005.

[6] Moniz, L., Search for extended air showers with TRC, in *Proceedings of the Sixth International Workshop on New Worlds in Astroparticle Physics*, 2007.