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R&D in photosensors and data acquisition systems for a new generation of Cosmic Ray Cherenkov and Fluorescence Imaging focal planes

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ABSTRACT

In this work we present the design, first prototypes and experimental R&D activities on the development of novel imaging cameras for Imaging Atmospheric Cherenkov and Fluorescence Telescopes. The baseline solution for the focal plane is based on a photosensor architecture instrumented with Silicon Photomultipliers (SiPMs). To decrease the trigger threshold and improve the signal-to-noise ratio for low-energy events, the Photon Counting technique is used. For very bright events the conventional Charge Integration approach is retained. The large number of channels requires a compact and modular design with minimal cabling and distance between the photosensors and the frontend. Other design requirements are an efficient light concentration system treated with an anti-reflective coating, a liquid cooling system able to keep the SiPMs at a temperature of $-20\,^{\circ}$C to $-10\,^{\circ}$C, a low-power frontend electronics down to 1 kW/m^2 and an easy field maintenance, high reliability data acquisition and trigger system. In the baseline design, the data acquisition system is partitioned in on-board frontend and off-detector high-level trigger electronics. Extensive use of mixed-signal ASICs and low-power FPGAs for early data reduction (Level 1 trigger), compatible with a liquid cooling sub-system for temperature control is adopted. The off-detector data acquisition and higher trigger (Level 2 and Level 3) architecture is based on the VME64X standard. The boards are connected by multi-Gbps optical links to the focal plane camera. Trigger primitives are sent asynchronously to the trigger boards via data links running at their own clocks. Data and slow-control data streams are also sent over the same links with the parallel VME64X backplane kept for trigger board configuration, slow-control and final data readout. Each 8-slot 6U crate can process up to about 3.6×10^4 SiPM channels.

1. Introduction

The development of a new generation of focal planes aims the improvement of the light detection efficiency, spatial and angular resolution of Cosmic Ray Air Cherenkov and Fluorescence Imaging Telescopes. Multi-pixel Geiger-mode APD, also called Silicon Photomultipliers (SiPMs) are considered as the baseline photosensor element since several of the already existing devices achieve better light detection efficiency, spatial and angular resolution than standard photomultiplier tubes. However, SiPMs still present a high level of dark current, after-pulsing and cross-talk [1]. Further optimizations of these parameters are in progress as a result of joint R&D programs with the industry. Due to the potential deployment of such focal planes in upgrades to the installed facilities at the Pierre Auger South [2,3] or in the future Cherenkov Telescope Array (CTA) [4], design principles such as the minimization of the total electrical power budget, high reliability and field maintenance with the lowest down-time achievable were considered.

The present paper is organized as following: in Section 2 the focal surface design and trigger architecture are described; in Section 3 the first prototypes of the focal plane demonstrator, readout electronics and experimental measurements are presented; finally a summary and a description of the future work is given.

2. Focal surface design and trigger architecture

The baseline focal plane surface adopts Silicon Photomultipliers [1,5] arrays with enhanced photon detection sensitivity in

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the 300–600 nm band, a fast temporal response and a spatial segmentation between 1 and 25 mm^2. For the backup solution, the Hamamatsu 64 Multi-Anode Photomultipliers (MA-PMT) was selected [6]. The mechanics and electronics interconnects of the entire system follows a modular approach, allowing to build smaller or even combine larger focal planes, while keeping the same frontend and data acquisition electronics. The increase on the number of photosensors due to the reduction of the pixel area leads to a larger number of active channels (10^4–10^5), requiring a compact and modular design with a minimum cabling and distance between the photosensors and the frontend electronics. A maximum power consumption of 1 kW per 1 m^2 focal plane is also mandatory in face of the restricted electrical budget available in most of the experimental sites.

Photosensors will operate in Photon Counting [7] in the low-light regime reverting to a charge integration approach in the presence of very intense light bursts. In Photon Counting mode, the effects of electronics noise and the SiPM or MA-PMT gain differences are kept negligible allowing to lower the photoelectron trigger threshold [7]. The focal surface is instrumented with 3×3 mm^2 SiPM pixels organized in 8×8 pixel arrays readout by a 64 input channel mixed-signal ASIC for Photon Counting in the low-light regime. The focal plane will be partitioned into independent Sectors. Each Sector corresponds to a total of 16 SiPM arrays (32×32 pixels) readout by a Level 1 board located on the focal plane backplane (Fig. 1).

Trigger primitives and data are sent to the Level 2 trigger (L2) which is housed in an off-detector VME64X crate. When working in air fluorescence detection mode, this trigger searches for persistent activity in a programmable time window. If a trigger accept is issued by the corresponding L2 board the time tag and channel identifier with the location of each active array is transmitted to the L3 board which performs the air fluorescence track identification. The binary image or count histograms are stored in temporary memory of the L2 board waiting for the L3 decision. In the L3 board, a pattern of five adjacent SiPM arrays overlapping during the coincidence time are accepted as valid trigger [8]. In this case, a L2 trigger accept is issued and data is moved to the L3 board where it is packaged for transmission to the acquisition computer via the VME64X Master Controller. Both the trigger primitives and the accepted data are moved to the off-detector electronics by means of multi-Gbps optical links.

3. First prototypes and experimental results

3.1. SiPM focal plane demonstrator

A focal plane technical demonstrator to test the feasibility of the Photon Counting technique with SiPMs was designed. This demonstrator consists of a SiPM array placed in thermal contact with a cooling copper plate enclosed in a gas-tight box (Fig. 2(a)). The gas-tight demonstrator can be flushed with N_2 gas, allowing it to be cooled down to -20 °C without the risk of water condensation. The copper plate is cooled by running ethylene glycol [9]. Fig. 2(b) shows a 3D view of the developed array of 4×4 SiPMs together with the light collecting Winston cones consisting of a high-reflectivity ($\geq 90\%$ from 300 to 700 nm) foil, designed by MPI-Munchen, glued into a plastic form. On the top side, the unit is closed by a high transmittance ($\geq 95\%$) optical entrance window. A calibrated HPD Hamamatsu R9792U-40 with a photocathode quantum efficiency of 32–34% at 360 nm [10] will also be installed near the SiPM array for calibration purposes.

3.2. SiPM single Photon Counting with MAROC3 ASIC

Feasibility tests to demonstrate the single Photon Counting of SiPM with current available ASICs were carried out. For this purpose, the MAROC3 ASIC developed by the OMEGA microelectronics group

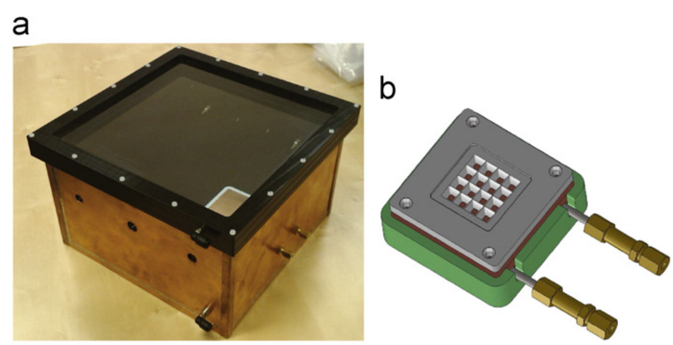

Fig. 2. (a) Photograph of the focal plane demonstrator and (b) 3D view of the 4×4 SiPM array equipped with a set of light collecting Winston cones mounted on top of the copper cooling plate.

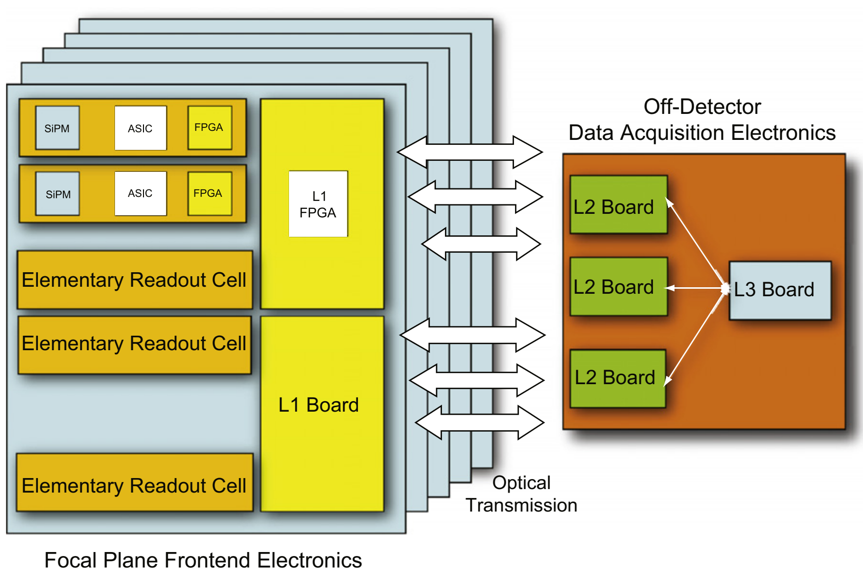

Fig. 1. Data acquisition and trigger system architecture.

was evaluated [11]. The MAROC3 is a 64 channel readout ASIC, designed in 0.35 μm AMS SiGe with a power consumption of 3.5 mW per channel. Each channel has a low impedance preamplifier with a variable gain setting (0 to 4 ×). Three different shapers can be used for each channel: unipolar (4.3 V/pC), bipolar (2.3 V/pC) and half-gain bipolar. The shaped pulse is compared against a threshold voltage set by the on-chip DAC.

Using the OMEGA MAROC3 evaluation board, Hamamatsu S10362-33-100C MPPCs operating at gain $M=2.4\times10^6$ (bias voltage of 70.67 V at room temperature 25 °C) placed in a PCB carrier board inside the focal plane demonstrator were readout (Fig. 3). Due to the large dark current of the $3\times3\ \mathrm{mm}^2$ MPPC (4–9 MHz) and the longer fall time of the 100 μm cells, a blocking capacitor of 220 pF was used to reduce the SiPM fall time down to 80 ns. The MAROC3 fast bipolar shaper (2.3 V/pC) was used. The discriminator output (Fig. 4) was connected to a CAEN N145 NIM counter. The threshold voltage of the discriminator was scanned and the number of counts recorded. At 0.5 photoelectron (p.e.) the dark count measured with the MAROC3 is 4.5–4.6 MHz in good agreement with the Hamamatsu value for this sample (4.8 MHz at 0.5 p.e.) (Fig. 5). The ratio of the dark count at 1.5 p.e. over the dark count at 0.5 p.e. measured with the MAROC3 was 17–20%.

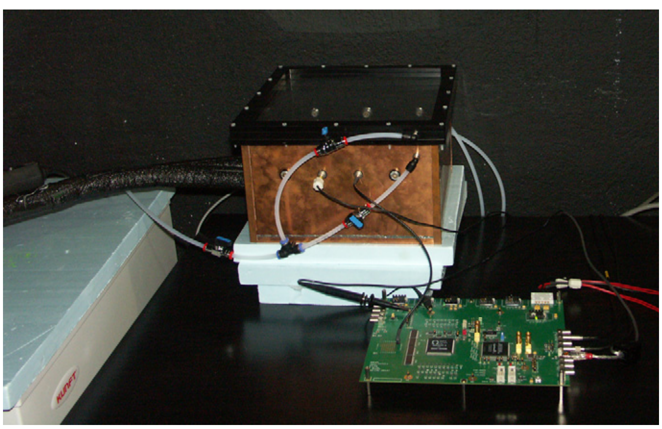

Fig. 3. Experimental test setup: liquid cooling system, N_2 flush system, OMEGA MAROC3 readout board connected to a S10362-33-100C MPPC pixel of the focal plane demonstrator.

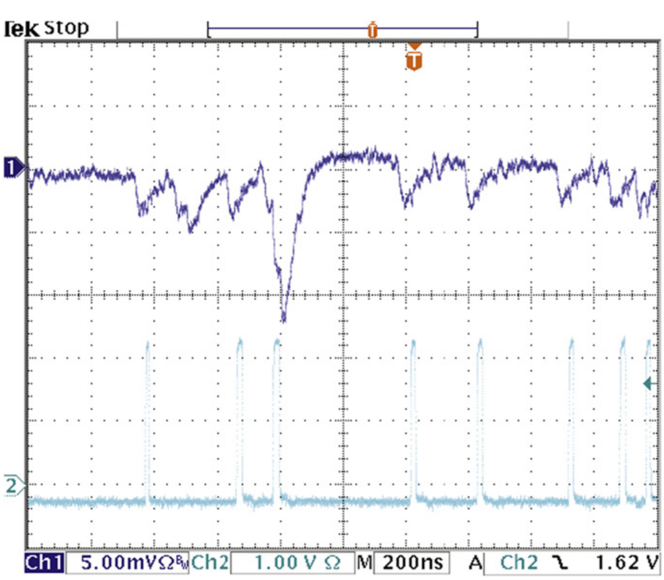

Fig. 4. Hamamatsu S10362-33-100C MPPC tests: typical oscilloscope traces of the MAROC3 fast preamplifier and discriminator output (room temperature 25 °C).

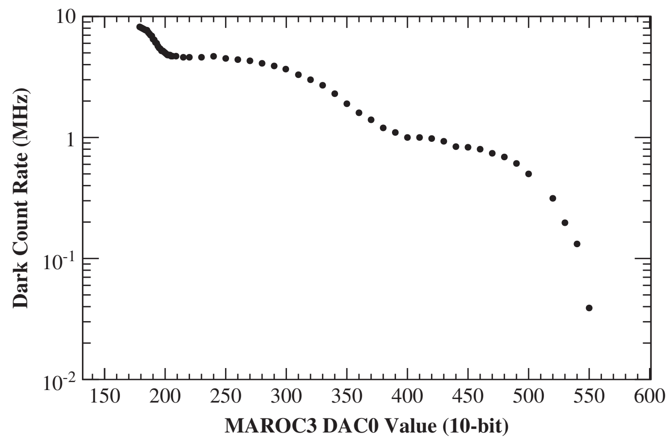

Fig. 5. Hamamatsu S10362-33-100C MPPC operated at 70.67 V (room temperature 25 °C) photoelectron dark count spectra.

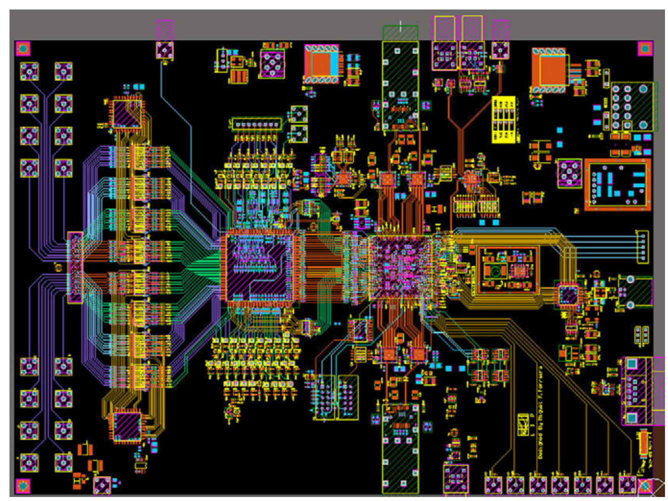

Fig. 6. Elementary Readout Cell (ERC) prototype board PCB layout.

Measurements at −14 °C were also made, with the bias voltage adjusted to yield pulses with similar amplitudes to those at 25 °C. At this temperature the dark count at 0.5 p.e. was 590 kHz.

3.3. Prototype frontend and Level 1 electronics board

A prototype board called ‘‘Elementary Readout Cell’’ is also under development with the aim to validate solutions for the main electronics sub-systems for the focal plane frontend and Level 1 trigger.

The main connector to the SiPM array is an 80-pin SMT connector with 16 SMA additional inputs for generic applications. In this prototype, the SiPM array is readout by the 64 channel MAROC3 ASIC. The 64 discriminator outputs as well as the 12-bit ADC serial datastream is readout by an EP3C80F780 Altera Cyclone III FPGA (Fig. 6). Valid data will be selected and concentrated in the FPGA following transmission to 3.125 Gbps 8b/10b SerDes chips connected to two 850 nm SFP optical modules. For debugging and slow-control purposes, a RS232 and a USB2 data links were also included. The FPGA is also responsible for monitoring the temperature and humidity, using dedicated I^2C sensors. Two 32-channel I^2C 0–5 V DACs are used to tune the individual SiPM bias. Two configuration schemes are employed: JTAG for direct configuration of the FPGA and Active Serial on system boot using the data stored on a EPCS device.

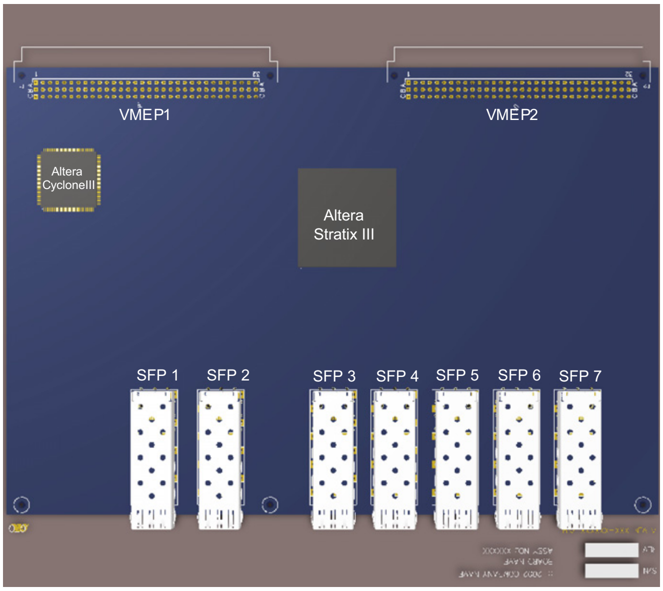

Fig. 7. 3D view of the 6U VME64X Level 2 and Level 3 trigger board during the pre-placement study phase.

The PCB interconnection has been distributed over 12-layer: top and bottom, five internal signal layers, three power planes (splitted into 0.75 V, 1.2 V, 1.5 V, 2.5 V, 3.3 V, 3.5 V regions) and two ground planes (digital and MAROC3 GND). Impedance controlled lines (50 and differential 100 Ohm pairs) in critical regions such as the MAROC3 inputs and the high speed SerDes were routed with priority over other signals, with the trace length, distance and PCB dielectric thickness selected in consultation with the manufacturer. LDO regulators were used with the exception of the 1.2 V (FPGA core) and 3.3 V voltages in which low-ripple, shielded DC/DC converters were selected. If required both DC/DC converters can be switched off and replaced by external linear supplies. The PCB will be submitted for production in July 2011 and the first validation tests are scheduled for September 2011.

3.4. Prototype Level 2 and Level 3 trigger board

A first prototype for the high-trigger board is being designed in a VME64X 6U Eurocard. The board is equipped with an Altera Stratix III FPGA, capable of receiving and transmitting data to and from seven 3.125 Gbps SFP optical links. Temporary storage is implemented in two 2 Gbyte DDR SRAM. An auxiliary Cyclone III FPGA implements the VME64X interface (Fig. 7). Different firmwares can be used in this board allowing to configure the board as a Level 2 or a Level 3 trigger. The boards will be housed on a VME64X crate, in which the backplane provides rear electrical interconnections dedicated to slow control and configuration. Up to 36,864 channels from a focal plane with 24×24 SiPM 64 pixel arrays can be handled by a 8-slot VME64X crate, in which 6 slots will be dedicated to Level 2 trigger boards, 1 slot for the Level 3 trigger board and the last slot for the VME64X Master Controller board. This configuration corresponds to a total surface area of about 1 m^2, which is equivalent to the already existing Air Fluorescence Telescopes used by the Pierre Auger Collaboration [3].

4. Summary and future work

In this paper, a concept for a new generation of focal planes and first feasibility tests were presented. Photon Counting and highly integrated frontend readout electronics allow to define a $1 \times 1\ m^2$ focal plane with a total power consumption no greater than 1 kW. Experimental work concerning the performance characterization of candidate SiPM pixels, as well as the development of a liquid cooling system and prototype frontend and data concentrator boards for the focal plane electronics have been initiated. The first experimental tests of the focal plane demonstrator using an array of 4×4 SiPMs are foreseen for late 2011.

Acknowledgments

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