TÉCNICO LISBOA

# Projecto e Controlo em Lógica Digital

www.lip.pt/~pedjor/PCLD

- Introdução
  - FPGAs
  - Laboratório
  - Verilog
  - Lógica combinatória
  - Lógica sequencial
- Máquinas estado
- Advanced verilog (video, etc.)

**Refs:**
Cyclone II device Handbook, Altera corp.
Quartus II Handbook , Altera corp.
DE2 documentation
Verilog HDL, S. Palnitkar, Prentice Hall

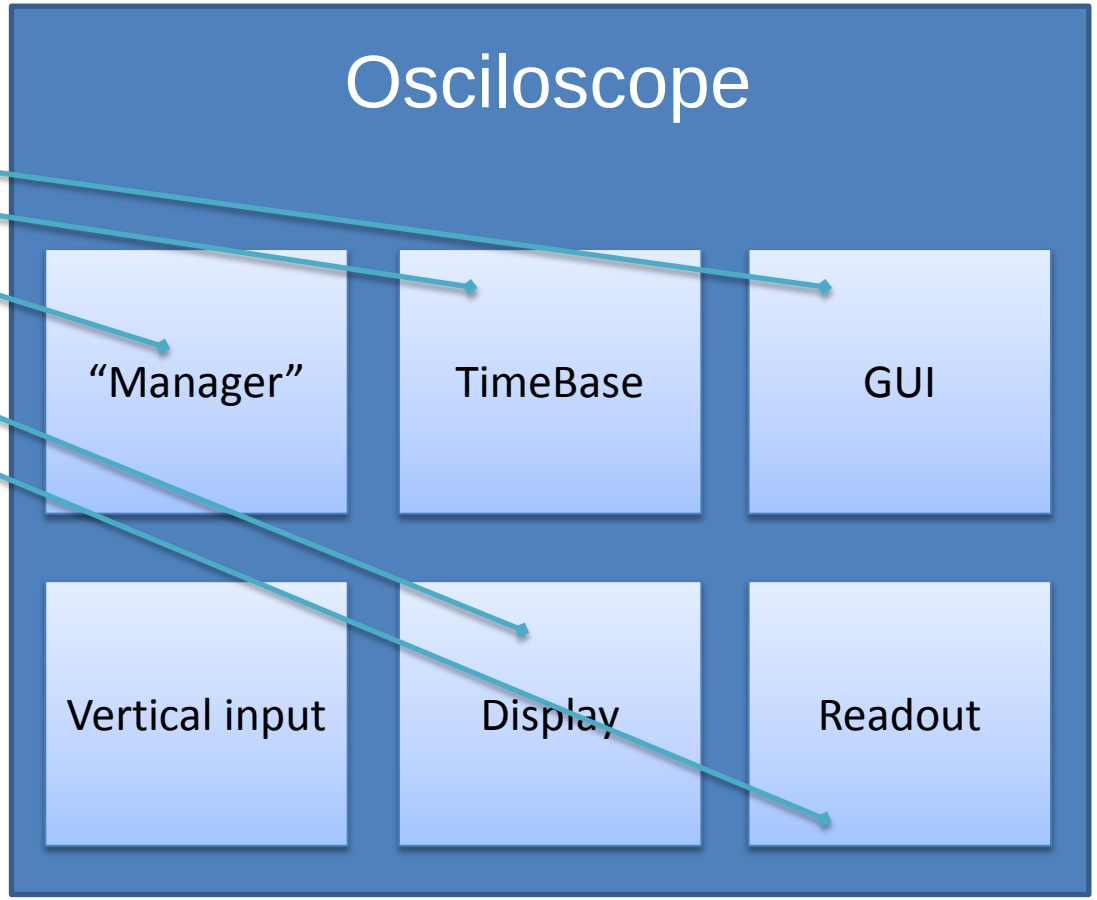
## Programação de Lógica Digital…



Inspired on course 6.111 from MIT * Some support material taken from 6.111 (thank you)

# Estrutura

Trabalhos:
Ex1: Ola Mundo
Ex2: Cronómetro
Ex3: Máquinas Estados
Ex4: Mira Técnica
Ex5: Microprocessor
T1: Osciloscópio
T2: à escolha / negociado



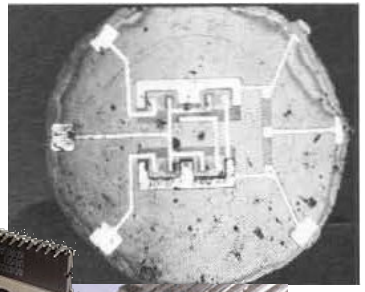

Avaliação

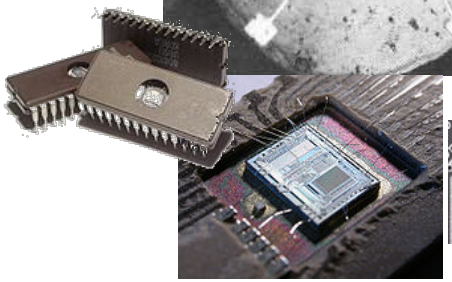
Exercícios avaliados em trinário (0,1,2); valem 25%
Trabalho 1: Avaliação 0-20; vale 25%
Trabalho2: Avaliação 0-20; vale 50%

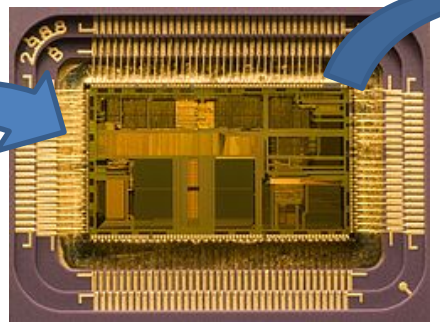
Nota= (Ex1+Ex2+Ex3+Ex4+Ex5)/5*10 *0.25+T1 * 0.25 + T2 * 0.5

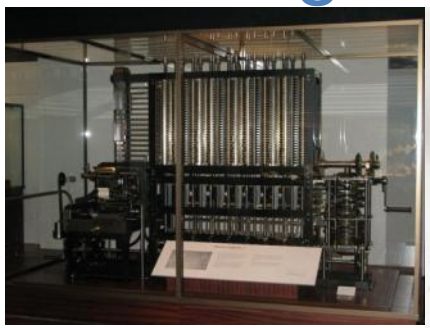
# Lógica Digital

# Programação

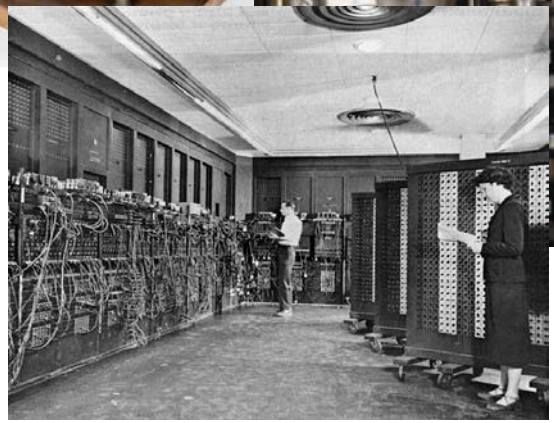




Babbage difference engine



# Lógica Digital de Programação?

Tudo funciona ou por magia ou com gnomos…

**Programação de microprocessadores**
(assembly, c++, etc.)

Dar ao "gnomo" uma lista (consecutiva) de operações a realizar

1 Máquina executa várias tarefas consecutivas

**Programação de Lógica Digital**
(FPGAs+HDL)

Dar ao gnomo uma lista de "objectos" para construir

Várias Máquinas executam várias tarefas em paralelo

Em linguagens de alto nível por vezes confundem-se

2+2?
Resultado x 2?

```
A=2+2
Cout << A
A=A*2
Cout << A
```

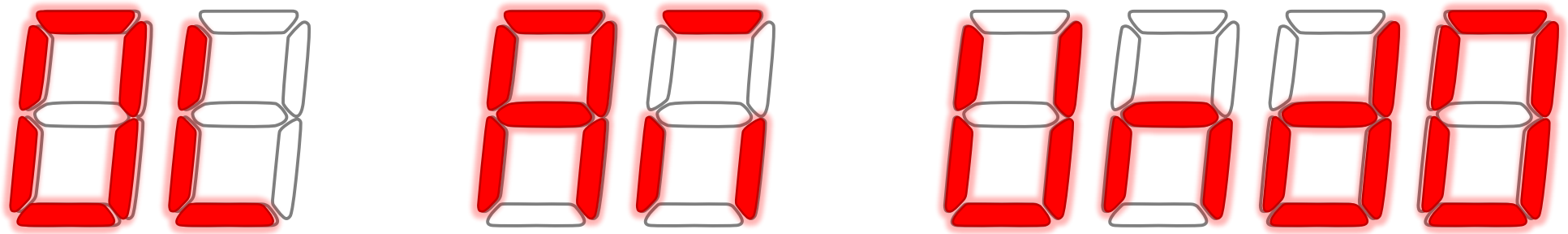
```
A=4
4!
A=8
8!
```

tempo

```
A=2+2
Output A
A=A*2
Output A
```

**Somador**: A=4
"ao mesmo tempo"
**Multiplicador:** A=A*2
Saída ??? (glitches?)

# Uma FPGA a funcionar...

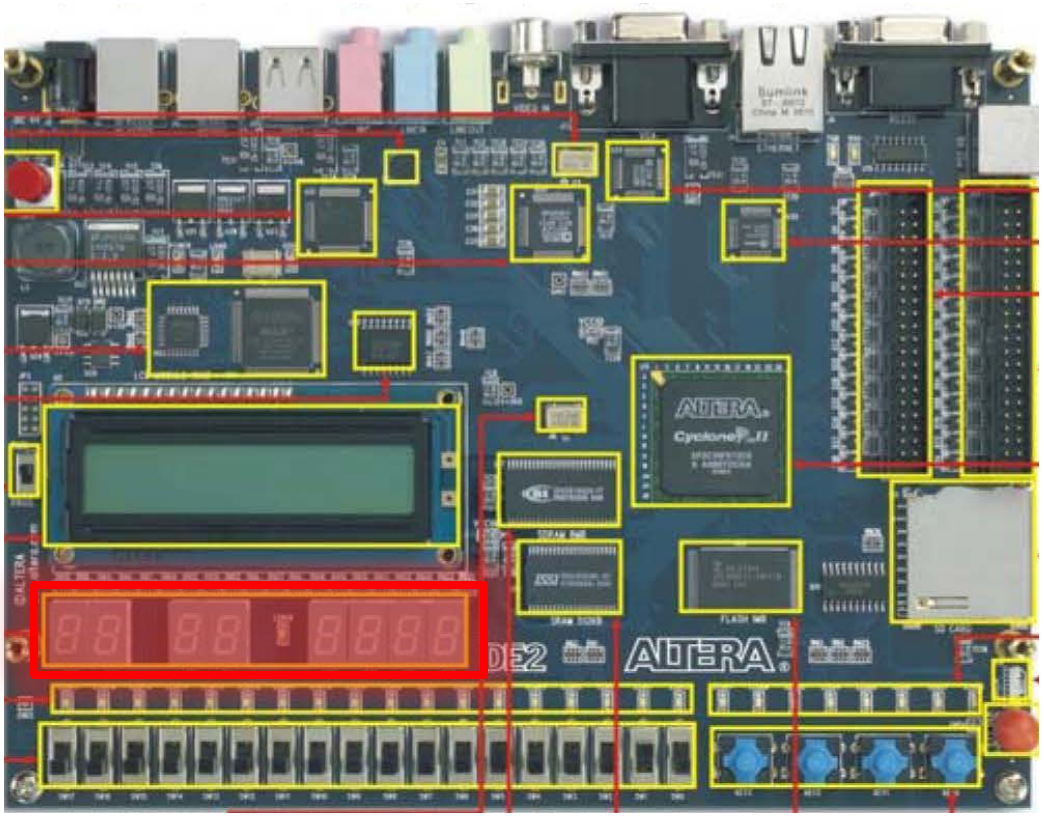


Primeiro exercício...

# Hardware


ALTERA DE2
Development and Education Board
Cyclone II
QUARTUS II

# Hardware



# Hardware

## DE2_Pin Table.pdf

Altera DE2 Board Pin Table

| Signal Name | FPGA Pin No. | Description |
|---|---|---|
| SW[0] | PIN_N25 | Toggle Switch[0] |
| SW[1] | PIN_N26 | Toggle Switch[1] |
| SW[2] | PIN_P25 | Toggle Switch[2] |
| SW[3] | PIN_AE14 | Toggle Switch[3] |
| SW[4] | PIN_AF14 | Toggle Switch[4] |
| SW[5] | PIN_AD13 | Toggle Switch[5] |
| SW[6] | PIN_AC13 | Toggle Switch[6] |
| SW[7] | PIN_C13 | Toggle Switch[7] |
| SW[8] | PIN_B13 | Toggle Switch[8] |
| SW[9] | PIN_A13 | Toggle Switch[9] |
| SW[10] | PIN_N1 | Toggle Switch[10] |
| SW[11] | PIN_P1 | Toggle Switch[11] |
| SW[12] | PIN_P2 | Toggle Switch[12] |
| SW[13] | PIN_T7 | Toggle Switch[13] |
| SW[14] | PIN_U3 | Toggle Switch[14] |
| SW[15] | PIN_U4 | Toggle Switch[15] |
| SW[16] | PIN_V1 | Toggle Switch[16] |
| SW[17] | PIN_V2 | Toggle Switch[17] |
| DRAM_ADDR[0] | PIN_T6 | SDRAM Address[0] |
| DRAM_ADDR[1] | PIN_V4 | SDRAM Address[1] |
| DRAM_ADDR[2] | PIN_V3 | SDRAM Address[2] |
| DRAM_ADDR[3] | PIN_W2 | SDRAM Address[3] |
| DRAM_ADDR[4] | PIN_W1 | SDRAM Address[4] |
| DRAM_ADDR[5] | PIN_U6 | SDRAM Address[5] |
| DRAM_ADDR[6] | PIN_U7 | SDRAM Address[6] |
| DRAM_ADDR[7] | PIN_U5 | SDRAM Address[7] |
| DRAM_ADDR[8] | PIN_W4 | SDRAM Address[8] |
| DRAM_ADDR[9] | PIN_W3 | SDRAM Address[9] |
| DRAM_ADDR[10] | PIN_Y1 | SDRAM Address[10] |
| DRAM_ADDR[11] | PIN_V5 | SDRAM Address[11] |
| DRAM_DQ[0] | PIN_V6 | SDRAM Data[0] |
| DRAM_DQ[1] | PIN_AA2 | SDRAM Data[1] |
| DRAM_DQ[2] | PIN_AA1 | SDRAM Data[2] |
| DRAM_DQ[3] | PIN_Y3 | SDRAM Data[3] |
| DRAM_DQ[4] | PIN_Y4 | SDRAM Data[4] |
| DRAM_DQ[5] | PIN_R8 | SDRAM Data[5] |
| DRAM_DQ[6] | PIN_T8 | SDRAM Data[6] |
| DRAM_DQ[7] | PIN_V7 | SDRAM Data[7] |
| DRAM_DQ[8] | PIN_W6 | SDRAM Data[8] |
| DRAM_DQ[9] | PIN_AB2 | SDRAM Data[9] |
| DRAM_DQ[10] | PIN_AB1 | SDRAM Data[10] |
| DRAM_DQ[11] | PIN_AA4 | SDRAM Data[11] |
| DRAM_DQ[12] | PIN_AA3 | SDRAM Data[12] |
| DRAM_DQ[13] | PIN_AC2 | SDRAM Data[13] |
| DRAM_DQ[14] | PIN_AC1 | SDRAM Data[14] |
| DRAM_DQ[15] | PIN_AA5 | SDRAM Data[15] |
| DRAM_BA_0 | PIN_AE2 | SDRAM Bank Address[0] |
| DRAM_BA_1 | PIN_AE3 | SDRAM Bank Address[1] |
| DRAM_LDQM | PIN_AD2 | SDRAM Low-byte Data Mask |
| DRAM_UDQM | PIN_Y5 | SDRAM High-byte Data Mask |
| DRAM_RAS_N | PIN_AB4 | SDRAM Row Address Strobe |
| DRAM_CAS_N | PIN_AB3 | SDRAM Column Address Strobe |
| DRAM_CKE | PIN_AA6 | SDRAM Clock Enable |
| DRAM_CLK | PIN_AA7 | SDRAM Clock |
| DRAM_WE_N | PIN_AD3 | SDRAM Write Enable |
| DRAM_CS_N | PIN_AC3 | SDRAM Chip Select |
| Signal Name | FPGA Pin No. | Description |
| FL_ADDR[0] | PIN_AC18 | FLASH Address[0] |
| FL_ADDR[1] | PIN_AB18 | FLASH Address[1] |
| FL_ADDR[2] | PIN_AE19 | FLASH Address[2] |
| FL_ADDR[3] | PIN_AF19 | FLASH Address[3] |
| FL_ADDR[4] | PIN_AE18 | FLASH Address[4] |

Altera DE2 Board Pin Table

| | | |
|---|---|---|
| FL_ADDR[5] | PIN_AF18 | FLASH Address[5] |
| FL_ADDR[6] | PIN_Y16 | FLASH Address[6] |
| FL_ADDR[7] | PIN_AA16 | FLASH Address[7] |
| FL_ADDR[8] | PIN_AD17 | FLASH Address[8] |
| FL_ADDR[9] | PIN_AC17 | FLASH Address[9] |
| FL_ADDR[10] | PIN_AE17 | FLASH Address[10] |
| FL_ADDR[11] | PIN_AF17 | FLASH Address[11] |
| FL_ADDR[12] | PIN_W16 | FLASH Address[12] |
| FL_ADDR[13] | PIN_W15 | FLASH Address[13] |
| FL_ADDR[14] | PIN_AC16 | FLASH Address[14] |
| FL_ADDR[15] | PIN_AD16 | FLASH Address[15] |
| FL_ADDR[16] | PIN_AE16 | FLASH Address[16] |
| FL_ADDR[17] | PIN_AC15 | FLASH Address[17] |
| FL_ADDR[18] | PIN_AB15 | FLASH Address[18] |
| FL_ADDR[19] | PIN_AA15 | FLASH Address[19] |
| FL_ADDR[20] | PIN_Y15 | FLASH Address[20] |
| FL_ADDR[21] | PIN_Y14 | FLASH Address[21] |
| FL_DQ[0] | PIN_AD19 | FLASH Data[0] |
| FL_DQ[1] | PIN_AC19 | FLASH Data[1] |
| FL_DQ[2] | PIN_AF20 | FLASH Data[2] |
| FL_DQ[3] | PIN_AE20 | FLASH Data[3] |
| FL_DQ[4] | PIN_AB20 | FLASH Data[4] |
| FL_DQ[5] | PIN_AC20 | FLASH Data[5] |
| FL_DQ[6] | PIN_AF21 | FLASH Data[6] |
| FL_DQ[7] | PIN_AE21 | FLASH Data[7] |
| FL_CE_N | PIN_V17 | FLASH Chip Enable |
| FL_OE_N | PIN_W17 | FLASH Output Enable |
| FL_RST_N | PIN_AA18 | FLASH Reset |
| FL_WE_N | PIN_AA17 | FLASH Write Enable |
| Signal Name | FPGA Pin No. | Description |
| SRAM_ADDR[0] | PIN_AE4 | SRAM Address[0] |
| SRAM_ADDR[1] | PIN_AF4 | SRAM Address[1] |
| SRAM_ADDR[2] | PIN_AC5 | SRAM Address[2] |
| SRAM_ADDR[3] | PIN_AC6 | SRAM Address[3] |
| SRAM_ADDR[4] | PIN_AD4 | SRAM Address[4] |
| SRAM_ADDR[5] | PIN_AD5 | SRAM Address[5] |
| SRAM_ADDR[6] | PIN_AE5 | SRAM Address[6] |
| SRAM_ADDR[7] | PIN_AF5 | SRAM Address[7] |
| SRAM_ADDR[8] | PIN_AC6 | SRAM Address[8] |
| SRAM_ADDR[9] | PIN_AD7 | SRAM Address[9] |
| SRAM_ADDR[10] | PIN_V10 | SRAM Address[10] |
| SRAM_ADDR[11] | PIN_V9 | SRAM Address[11] |
| SRAM_ADDR[12] | PIN_AC7 | SRAM Address[12] |
| SRAM_ADDR[13] | PIN_W8 | SRAM Address[13] |
| SRAM_ADDR[14] | PIN_W10 | SRAM Address[14] |
| SRAM_ADDR[15] | PIN_Y10 | SRAM Address[15] |
| SRAM_ADDR[16] | PIN_AB8 | SRAM Address[16] |
| SRAM_ADDR[17] | PIN_AC8 | SRAM Address[17] |
| SRAM_DQ[0] | PIN_AD8 | SRAM Data[0] |
| SRAM_DQ[1] | PIN_AE6 | SRAM Data[1] |
| SRAM_DQ[2] | PIN_AF6 | SRAM Data[2] |
| SRAM_DQ[3] | PIN_AA9 | SRAM Data[3] |
| SRAM_DQ[4] | PIN_AA10 | SRAM Data[4] |
| SRAM_DQ[5] | PIN_AB10 | SRAM Data[5] |
| SRAM_DQ[6] | PIN_AA11 | SRAM Data[6] |
| SRAM_DQ[7] | PIN_Y11 | SRAM Data[7] |
| SRAM_DQ[8] | PIN_AE7 | SRAM Data[8] |
| SRAM_DQ[9] | PIN_AF7 | SRAM Data[9] |
| SRAM_DQ[10] | PIN_AE8 | SRAM Data[10] |
| SRAM_DQ[11] | PIN_AF8 | SRAM Data[11] |
| SRAM_DQ[12] | PIN_W11 | SRAM Data[12] |
| SRAM_DQ[13] | PIN_W12 | SRAM Data[13] |
| SRAM_DQ[14] | PIN_AC9 | SRAM Data[14] |
| SRAM_DQ[15] | PIN_AC10 | SRAM Data[15] |

Altera DE2 Board Pin Table

| | | |
|---|---|---|
| SRAM_WE_N | PIN_AE10 | SRAM Write Enable |
| SRAM_OE_N | PIN_AD10 | SRAM Output Enable |
| SRAM_UB_N | PIN_AF9 | SRAM High-byte Data Mask |
| SRAM_LB_N | PIN_AE9 | SRAM Low-byte Data Mask |
| SRAM_CE_N | PIN_AC11 | SRAM Chip Enable |
| Signal Name | FPGA Pin No. | Description |
| OTG_ADDR[0] | PIN_K7 | ISP1362 Address[0] |
| OTG_ADDR[1] | PIN_F2 | ISP1362 Address[1] |
| OTG_DATA[0] | PIN_F4 | ISP1362 Data[0] |
| OTG_DATA[1] | PIN_D2 | ISP1362 Data[1] |
| OTG_DATA[2] | PIN_D1 | ISP1362 Data[2] |
| OTG_DATA[3] | PIN_F7 | ISP1362 Data[3] |
| OTG_DATA[4] | PIN_J5 | ISP1362 Data[4] |
| OTG_DATA[5] | PIN_J8 | ISP1362 Data[5] |
| OTG_DATA[6] | PIN_J7 | ISP1362 Data[6] |
| OTG_DATA[7] | PIN_H6 | ISP1362 Data[7] |
| OTG_DATA[8] | PIN_E2 | ISP1362 Data[8] |
| OTG_DATA[9] | PIN_E1 | ISP1362 Data[9] |
| OTG_DATA[10] | PIN_K6 | ISP1362 Data[10] |
| OTG_DATA[11] | PIN_K5 | ISP1362 Data[11] |
| OTG_DATA[12] | PIN_G4 | ISP1362 Data[12] |
| OTG_DATA[13] | PIN_G3 | ISP1362 Data[13] |
| OTG_DATA[14] | PIN_J6 | ISP1362 Data[14] |
| OTG_DATA[15] | PIN_K8 | ISP1362 Data[15] |
| OTG_CS_N | PIN_F1 | ISP1362 Chip Select |
| OTG_RD_N | PIN_G2 | ISP1362 Read |
| OTG_WR_N | PIN_G1 | ISP1362 Write |
| OTG_RST_N | PIN_G5 | ISP1362 Reset |
| OTG_INT0 | PIN_B3 | ISP1362 Interrupt 0 |
| OTG_INT1 | PIN_C3 | ISP1362 Interrupt 1 |
| OTG_DACK0_N | PIN_C2 | ISP1362 DMA Acknowledge 0 |
| OTG_DACK1_N | PIN_B2 | ISP1362 DMA Acknowledge 1 |
| OTG_DREQ0 | PIN_F6 | ISP1362 DMA Request 0 |
| OTG_DREQ1 | PIN_E5 | ISP1362 DMA Request 1 |
| OTG_FSPEED | PIN_F3 | USB Full Speed, 0 = Enable, Z = Disable |
| OTG_LSPEED | PIN_G6 | USB Low Speed, 0 = Enable, Z = Disable |
| Signal Name | FPGA Pin No. | Description |
| LCD_DATA[0] | PIN_J1 | LCD Data[0] |
| LCD_DATA[1] | PIN_J2 | LCD Data[1] |
| LCD_DATA[2] | PIN_H1 | LCD Data[2] |
| LCD_DATA[3] | PIN_H2 | LCD Data[3] |
| LCD_DATA[4] | PIN_J4 | LCD Data[4] |
| LCD_DATA[5] | PIN_J3 | LCD Data[5] |
| LCD_DATA[6] | PIN_H4 | LCD Data[6] |
| LCD_DATA[7] | PIN_H3 | LCD Data[7] |
| LCD_RW | PIN_K4 | LCD Read/Write Select, 0 = Write, 1 = Read |
| LCD_EN | PIN_K3 | LCD Enable |
| LCD_RS | PIN_K1 | LCD Command/Data Select, 0 = Command, 1 = Data |
| LCD_ON | PIN_L4 | LCD Power ON/OFF |
| LCD_BLON | PIN_K2 | LCD Back Light ON/OFF |
| Signal Name | FPGA Pin No. | Description |
| SD_DAT | PIN_AD24 | SD Card Data |
| SD_DAT3 | PIN_AC23 | SD Card Data 3 |
| SD_CMD | PIN_Y21 | SD Card Command Signal |
| SD_CLK | PIN_AD25 | SD Card Clock |
| Signal Name | FPGA Pin No. | Description |
| TDI | PIN_B14 | CPLD -> FPGA (Data in) |
| TCS | PIN_A14 | CPLD -> FPGA (CS) |
| TCK | PIN_D14 | CPLD -> FPGA (Clock) |
| TDO | PIN_F14 | FPGA -> CPLD (Data out) |
| Signal Name | FPGA Pin No. | Description |
| IRDA_TXD | PIN_AE24 | IRDA Transmitter |
| IRDA_RXD | PIN_AE25 | IRDA Receiver |
| Signal Name | FPGA Pin No. | Description |

Altera DE2 Board Pin Table

| | | |
|---|---|---|
| HEX0[0] | PIN_AF10 | Seven Segment Digit 0[0] |
| HEX0[1] | PIN_AB12 | Seven Segment Digit 0[1] |
| HEX0[2] | PIN_AC12 | Seven Segment Digit 0[2] |
| HEX0[3] | PIN_AD11 | Seven Segment Digit 0[3] |
| HEX0[4] | PIN_AE11 | Seven Segment Digit 0[4] |
| HEX0[5] | PIN_V14 | Seven Segment Digit 0[5] |
| HEX0[6] | PIN_V13 | Seven Segment Digit 0[6] |
| HEX1[0] | PIN_V20 | Seven Segment Digit 1[0] |
| HEX1[1] | PIN_V21 | Seven Segment Digit 1[1] |
| HEX1[2] | PIN_W21 | Seven Segment Digit 1[2] |
| HEX1[3] | PIN_Y22 | Seven Segment Digit 1[3] |
| HEX1[4] | PIN_AA24 | Seven Segment Digit 1[4] |
| HEX1[5] | PIN_AA23 | Seven Segment Digit 1[5] |
| HEX1[6] | PIN_AB24 | Seven Segment Digit 1[6] |
| HEX2[0] | PIN_AB23 | Seven Segment Digit 2[0] |
| HEX2[1] | PIN_V22 | Seven Segment Digit 2[1] |
| HEX2[2] | PIN_AC25 | Seven Segment Digit 2[2] |
| HEX2[3] | PIN_AC26 | Seven Segment Digit 2[3] |
| HEX2[4] | PIN_AB26 | Seven Segment Digit 2[4] |
| HEX2[5] | PIN_AB25 | Seven Segment Digit 2[5] |
| HEX2[6] | PIN_Y24 | Seven Segment Digit 2[6] |
| HEX3[0] | PIN_Y23 | Seven Segment Digit 3[0] |
| HEX3[1] | PIN_AA25 | Seven Segment Digit 3[1] |
| HEX3[2] | PIN_AA26 | Seven Segment Digit 3[2] |
| HEX3[3] | PIN_Y26 | Seven Segment Digit 3[3] |
| HEX3[4] | PIN_Y25 | Seven Segment Digit 3[4] |
| HEX3[5] | PIN_U22 | Seven Segment Digit 3[5] |
| HEX3[6] | PIN_W24 | Seven Segment Digit 3[6] |
| HEX4[0] | PIN_U9 | Seven Segment Digit 4[0] |
| HEX4[1] | PIN_U1 | Seven Segment Digit 4[1] |
| HEX4[2] | PIN_U2 | Seven Segment Digit 4[2] |
| HEX4[3] | PIN_T4 | Seven Segment Digit 4[3] |
| HEX4[4] | PIN_R7 | Seven Segment Digit 4[4] |
| HEX4[5] | PIN_R6 | Seven Segment Digit 4[5] |
| HEX4[6] | PIN_T3 | Seven Segment Digit 4[6] |
| HEX5[0] | PIN_T2 | Seven Segment Digit 5[0] |
| HEX5[1] | PIN_P6 | Seven Segment Digit 5[1] |
| HEX5[2] | PIN_P7 | Seven Segment Digit 5[2] |
| HEX5[3] | PIN_T9 | Seven Segment Digit 5[3] |
| HEX5[4] | PIN_R5 | Seven Segment Digit 5[4] |
| HEX5[5] | PIN_R4 | Seven Segment Digit 5[5] |
| HEX5[6] | PIN_R3 | Seven Segment Digit 5[6] |
| HEX6[0] | PIN_R2 | Seven Segment Digit 6[0] |
| HEX6[1] | PIN_P4 | Seven Segment Digit 6[1] |
| HEX6[2] | PIN_P3 | Seven Segment Digit 6[2] |
| HEX6[3] | PIN_M2 | Seven Segment Digit 6[3] |
| HEX6[4] | PIN_M3 | Seven Segment Digit 6[4] |
| HEX6[5] | PIN_M5 | Seven Segment Digit 6[5] |
| HEX6[6] | PIN_M4 | Seven Segment Digit 6[6] |
| HEX7[0] | PIN_L3 | Seven Segment Digit 7[0] |
| HEX7[1] | PIN_L2 | Seven Segment Digit 7[1] |
| HEX7[2] | PIN_L9 | Seven Segment Digit 7[2] |
| HEX7[3] | PIN_L6 | Seven Segment Digit 7[3] |
| HEX7[4] | PIN_L7 | Seven Segment Digit 7[4] |
| HEX7[5] | PIN_P9 | Seven Segment Digit 7[5] |
| HEX7[6] | PIN_N9 | Seven Segment Digit 7[6] |
| Signal Name | FPGA Pin No. | Description |
| KEY[0] | PIN_G26 | Pushbutton[0] |
| KEY[1] | PIN_N23 | Pushbutton[1] |
| KEY[2] | PIN_P23 | Pushbutton[2] |
| KEY[3] | PIN_W26 | Pushbutton[3] |
| Signal Name | FPGA Pin No. | Description |
| LEDR[0] | PIN_AE23 | LED Red[0] |
| LEDR[1] | PIN_AF23 | LED Red[1] |

SW[15] PIN_U4 Toggle Switch[15]

Altera DE2 Board Pin Table

| | | |
|---|---|---|
| LEDR[2] | PIN_AB21 | LED Red[2] |
| LEDR[3] | PIN_AC22 | LED Red[3] |
| LEDR[4] | PIN_AD22 | LED Red[4] |
| LEDR[5] | PIN_AD23 | LED Red[5] |
| LEDR[6] | PIN_AD21 | LED Red[6] |
| LEDR[7] | PIN_AC21 | LED Red[7] |
| LEDR[8] | PIN_AA14 | LED Red[8] |
| LEDR[9] | PIN_Y13 | LED Red[9] |
| LEDR[10] | PIN_AA13 | LED Red[10] |
| LEDR[11] | PIN_AC14 | LED Red[11] |
| LEDR[12] | PIN_AD15 | LED Red[12] |
| LEDR[13] | PIN_AE15 | LED Red[13] |
| LEDR[14] | PIN_AF13 | LED Red[14] |
| LEDR[15] | PIN_AE13 | LED Red[15] |
| LEDR[16] | PIN_AE12 | LED Red[16] |
| LEDR[17] | PIN_AD12 | LED Red[17] |
| LEDG[0] | PIN_AE22 | LED Green[0] |
| LEDG[1] | PIN_AF22 | LED Green[1] |
| LEDG[2] | PIN_W19 | LED Green[2] |
| LEDG[3] | PIN_V18 | LED Green[3] |
| LEDG[4] | PIN_U18 | LED Green[4] |
| LEDG[5] | PIN_U17 | LED Green[5] |
| LEDG[6] | PIN_AA20 | LED Green[6] |
| LEDG[7] | PIN_Y18 | LED Green[7] |
| LEDG[8] | PIN_Y19 | LED Green[8] |
| Signal Name | FPGA Pin No. | Description |
| CLOCK_27 | PIN_D13 | On Board 27 MHz |
| CLOCK_50 | PIN_N2 | On Board 50 MHz |
| EXT_CLOCK | PIN_P26 | External Clock |
| Signal Name | FPGA Pin No. | Description |
| UART_RXD | PIN_C25 | UART Receiver |
| UART_TXD | PIN_B25 | UART Transmitter |
| Signal Name | FPGA Pin No. | Description |
| PS2_CLK | PIN_D26 | PS2 Data |
| PS2_DAT | PIN_C24 | PS2 Clock |
| Signal Name | FPGA Pin No. | Description |
| I2C_SCLK | PIN_A6 | I2C Data |
| I2C_SDAT | PIN_B6 | I2C Clock |
| Signal Name | FPGA Pin No. | Description |
| TD_DATA[0] | PIN_J9 | TV Decoder Data[0] |
| TD_DATA[1] | PIN_E8 | TV Decoder Data[1] |
| TD_DATA[2] | PIN_H8 | TV Decoder Data[2] |
| TD_DATA[3] | PIN_H10 | TV Decoder Data[3] |
| TD_DATA[4] | PIN_G9 | TV Decoder Data[4] |
| TD_DATA[5] | PIN_F9 | TV Decoder Data[5] |
| TD_DATA[6] | PIN_D7 | TV Decoder Data[6] |
| TD_DATA[7] | PIN_C7 | TV Decoder Data[7] |
| TD_HS | PIN_D6 | TV Decoder H_SYNC |
| TD_VS | PIN_K9 | TV Decoder V_SYNC |
| TD_RESET | PIN_C4 | TV Decoder Reset |
| Signal Name | FPGA Pin No. | Description |
| VGA_R[0] | PIN_C8 | VGA Red[0] |
| VGA_R[1] | PIN_F10 | VGA Red[1] |
| VGA_R[2] | PIN_G10 | VGA Red[2] |
| VGA_R[3] | PIN_D9 | VGA Red[3] |
| VGA_R[4] | PIN_C9 | VGA Red[4] |
| VGA_R[5] | PIN_A8 | VGA Red[5] |
| VGA_R[6] | PIN_H11 | VGA Red[6] |
| VGA_R[7] | PIN_H12 | VGA Red[7] |
| VGA_R[8] | PIN_F11 | VGA Red[8] |
| VGA_R[9] | PIN_E10 | VGA Red[9] |
| VGA_G[0] | PIN_B9 | VGA Green[0] |
| VGA_G[1] | PIN_A9 | VGA Green[1] |
| VGA_G[2] | PIN_C10 | VGA Green[2] |

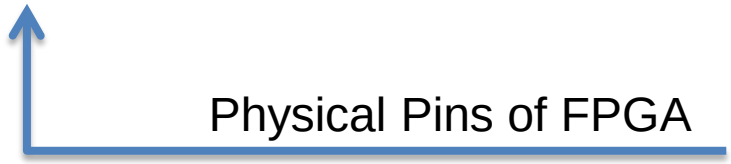
Altera DE2 Board Pin Table

| | | |
|---|---|---|
| VGA_G[3] | PIN_D10 | VGA Green[3] |
| VGA_G[4] | PIN_B10 | VGA Green[4] |
| VGA_G[5] | PIN_A10 | VGA Green[5] |
| VGA_G[6] | PIN_D11 | VGA Green[6] |
| VGA_G[7] | PIN_D11 | VGA Green[7] |
| VGA_G[8] | PIN_E12 | VGA Green[8] |
| VGA_G[9] | PIN_D12 | VGA Green[9] |
| VGA_B[0] | PIN_J13 | VGA Blue[0] |
| VGA_B[1] | PIN_J14 | VGA Blue[1] |
| VGA_B[2] | PIN_F12 | VGA Blue[2] |
| VGA_B[3] | PIN_G12 | VGA Blue[3] |
| VGA_B[4] | PIN_J10 | VGA Blue[4] |
| VGA_B[5] | PIN_J11 | VGA Blue[5] |
| VGA_B[6] | PIN_C11 | VGA Blue[6] |
| VGA_B[7] | PIN_B11 | VGA Blue[7] |
| VGA_B[8] | PIN_C12 | VGA Blue[8] |
| VGA_B[9] | PIN_B12 | VGA Blue[9] |
| VGA_CLK | PIN_B8 | VGA Clock |
| VGA_BLANK | PIN_D6 | VGA BLANK |
| VGA_HS | PIN_A7 | VGA H_SYNC |
| VGA_VS | PIN_D8 | VGA V_SYNC |
| VGA_SYNC | PIN_B7 | VGA SYNC |
| Signal Name | FPGA Pin No. | Description |
| AUD_ADCLRCK | PIN_C5 | Audio CODEC ADC LR Clock |
| AUD_ADCDAT | PIN_B5 | Audio CODEC ADC Data |
| AUD_DACLRCK | PIN_C6 | Audio CODEC DAC LR Clock |
| AUD_DACDAT | PIN_A4 | Audio CODEC DAC Data |
| AUD_XCK | PIN_A5 | Audio CODEC Chip Clock |
| AUD_BCLK | PIN_B4 | Audio CODEC Bit-Stream Clock |
| Signal Name | FPGA Pin No. | Description |
| ENET_DATA[0] | PIN_D17 | DM9000A DATA[0] |
| ENET_DATA[1] | PIN_C17 | DM9000A DATA[1] |
| ENET_DATA[2] | PIN_B18 | DM9000A DATA[2] |
| ENET_DATA[3] | PIN_A18 | DM9000A DATA[3] |
| ENET_DATA[4] | PIN_B17 | DM9000A DATA[4] |
| ENET_DATA[5] | PIN_A17 | DM9000A DATA[5] |
| ENET_DATA[6] | PIN_B16 | DM9000A DATA[6] |
| ENET_DATA[7] | PIN_B15 | DM9000A DATA[7] |
| ENET_DATA[8] | PIN_B20 | DM9000A DATA[8] |
| ENET_DATA[9] | PIN_A20 | DM9000A DATA[9] |
| ENET_DATA[10] | PIN_C19 | DM9000A DATA[10] |
| ENET_DATA[11] | PIN_D19 | DM9000A DATA[11] |
| ENET_DATA[12] | PIN_B19 | DM9000A DATA[12] |
| ENET_DATA[13] | PIN_A19 | DM9000A DATA[13] |
| ENET_DATA[14] | PIN_E18 | DM9000A DATA[14] |
| ENET_DATA[15] | PIN_D18 | DM9000A DATA[15] |
| ENET_CLK | PIN_B24 | DM9000A Clock 25 MHz |
| ENET_CMD | PIN_A21 | DM9000A Command/Data Select, 0 = Command, 1 = Data |
| ENET_CS_N | PIN_A23 | DM9000A Chip Select |
| ENET_INT | PIN_B21 | DM9000A Interrupt |
| ENET_RD_N | PIN_A22 | DM9000A Read |
| ENET_WR_N | PIN_B22 | DM9000A Write |
| ENET_RST_N | PIN_B23 | DM9000A Reset |
| Signal Name | FPGA Pin No. | Description |
| GPIO_0[0] | PIN_D25 | GPIO Connection 0[0] |
| GPIO_0[1] | PIN_J22 | GPIO Connection 0[1] |
| GPIO_0[2] | PIN_E26 | GPIO Connection 0[2] |
| GPIO_0[3] | PIN_E25 | GPIO Connection 0[3] |
| GPIO_0[4] | PIN_F24 | GPIO Connection 0[4] |
| GPIO_0[5] | PIN_F23 | GPIO Connection 0[5] |
| GPIO_0[6] | PIN_J21 | GPIO Connection 0[6] |
| GPIO_0[7] | PIN_J20 | GPIO Connection 0[7] |
| GPIO_0[8] | PIN_F25 | GPIO Connection 0[8] |
| GPIO_0[9] | PIN_F26 | GPIO Connection 0[9] |

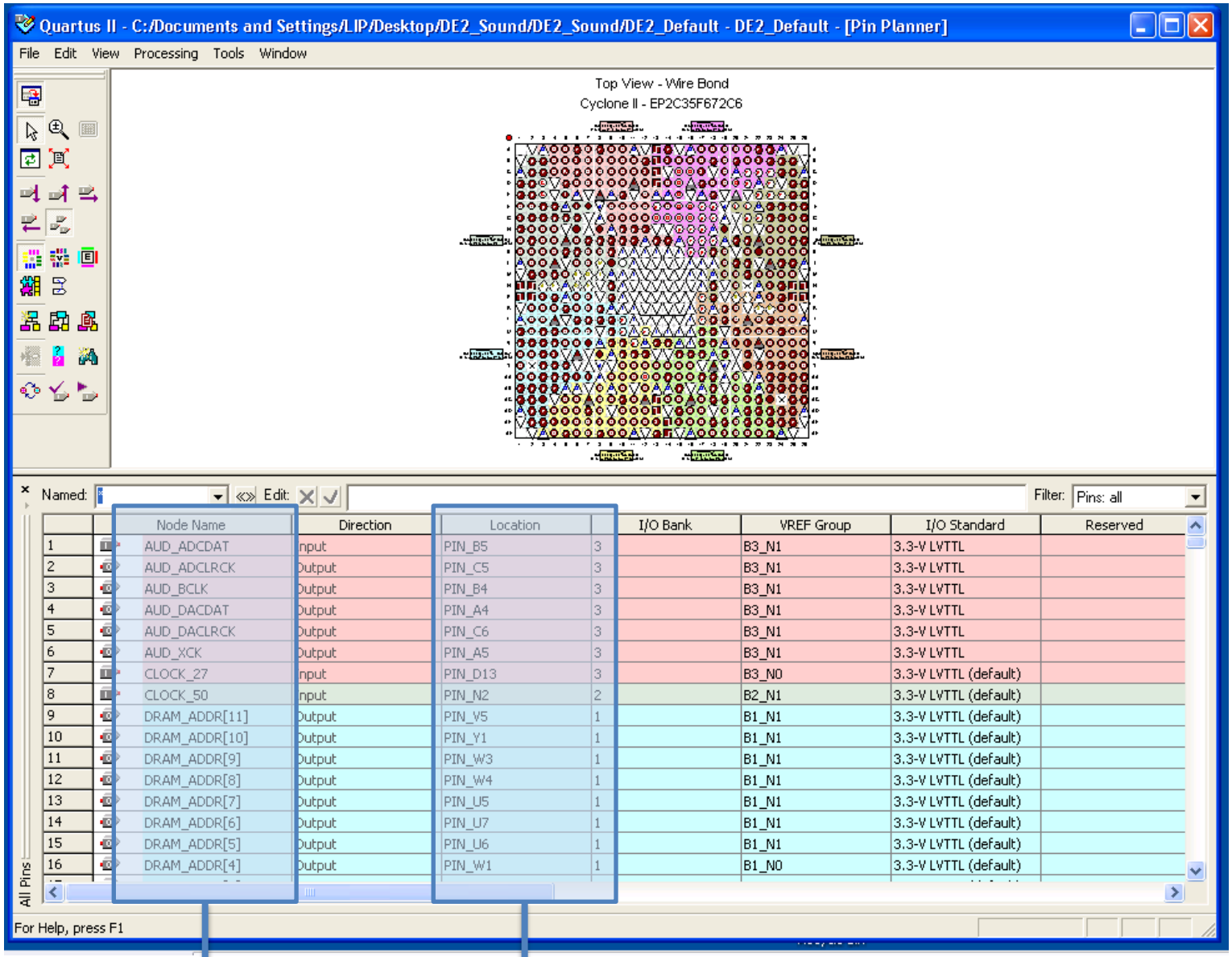
Altera DE2 Board Pin Table

| | | |
|---|---|---|
| GPIO_0[10] | PIN_N18 | GPIO Connection 0[10] |
| GPIO_0[11] | PIN_P18 | GPIO Connection 0[11] |
| GPIO_0[12] | PIN_G23 | GPIO Connection 0[12] |
| GPIO_0[13] | PIN_G24 | GPIO Connection 0[13] |
| GPIO_0[14] | PIN_K22 | GPIO Connection 0[14] |
| GPIO_0[15] | PIN_G25 | GPIO Connection 0[15] |
| GPIO_0[16] | PIN_H23 | GPIO Connection 0[16] |
| GPIO_0[17] | PIN_H24 | GPIO Connection 0[17] |
| GPIO_0[18] | PIN_J23 | GPIO Connection 0[18] |
| GPIO_0[19] | PIN_J24 | GPIO Connection 0[19] |
| GPIO_0[20] | PIN_H25 | GPIO Connection 0[20] |
| GPIO_0[21] | PIN_H26 | GPIO Connection 0[21] |
| GPIO_0[22] | PIN_H19 | GPIO Connection 0[22] |
| GPIO_0[23] | PIN_K19 | GPIO Connection 0[23] |
| GPIO_0[24] | PIN_K19 | GPIO Connection 0[24] |
| GPIO_0[25] | PIN_K21 | GPIO Connection 0[25] |
| GPIO_0[26] | PIN_K23 | GPIO Connection 0[26] |
| GPIO_0[27] | PIN_K24 | GPIO Connection 0[27] |
| GPIO_0[28] | PIN_L21 | GPIO Connection 0[28] |
| GPIO_0[29] | PIN_L20 | GPIO Connection 0[29] |
| GPIO_0[30] | PIN_J25 | GPIO Connection 0[30] |
| GPIO_0[31] | PIN_J26 | GPIO Connection 0[31] |
| GPIO_0[32] | PIN_L23 | GPIO Connection 0[32] |
| GPIO_0[33] | PIN_L24 | GPIO Connection 0[33] |
| GPIO_0[34] | PIN_L25 | GPIO Connection 0[34] |
| GPIO_0[35] | PIN_L19 | GPIO Connection 0[35] |
| GPIO_1[0] | PIN_K25 | GPIO Connection 1[0] |
| GPIO_1[1] | PIN_K26 | GPIO Connection 1[1] |
| GPIO_1[2] | PIN_M22 | GPIO Connection 1[2] |
| GPIO_1[3] | PIN_M23 | GPIO Connection 1[3] |
| GPIO_1[4] | PIN_M19 | GPIO Connection 1[4] |
| GPIO_1[5] | PIN_M20 | GPIO Connection 1[5] |
| GPIO_1[6] | PIN_N20 | GPIO Connection 1[6] |
| GPIO_1[7] | PIN_M21 | GPIO Connection 1[7] |
| GPIO_1[8] | PIN_M24 | GPIO Connection 1[8] |
| GPIO_1[9] | PIN_M25 | GPIO Connection 1[9] |
| GPIO_1[10] | PIN_N24 | GPIO Connection 1[10] |
| GPIO_1[11] | PIN_P24 | GPIO Connection 1[11] |
| GPIO_1[12] | PIN_R25 | GPIO Connection 1[12] |
| GPIO_1[13] | PIN_R24 | GPIO Connection 1[13] |
| GPIO_1[14] | PIN_R20 | GPIO Connection 1[14] |
| GPIO_1[15] | PIN_T22 | GPIO Connection 1[15] |
| GPIO_1[16] | PIN_T23 | GPIO Connection 1[16] |
| GPIO_1[17] | PIN_T24 | GPIO Connection 1[17] |
| GPIO_1[18] | PIN_T25 | GPIO Connection 1[18] |
| GPIO_1[19] | PIN_T18 | GPIO Connection 1[19] |
| GPIO_1[20] | PIN_T21 | GPIO Connection 1[20] |
| GPIO_1[21] | PIN_T20 | GPIO Connection 1[21] |
| GPIO_1[22] | PIN_U26 | GPIO Connection 1[22] |
| GPIO_1[23] | PIN_U25 | GPIO Connection 1[23] |
| GPIO_1[24] | PIN_U23 | GPIO Connection 1[24] |
| GPIO_1[25] | PIN_U24 | GPIO Connection 1[25] |
| GPIO_1[26] | PIN_R19 | GPIO Connection 1[26] |
| GPIO_1[27] | PIN_T19 | GPIO Connection 1[27] |
| GPIO_1[28] | PIN_U20 | GPIO Connection 1[28] |
| GPIO_1[29] | PIN_U21 | GPIO Connection 1[29] |
| GPIO_1[30] | PIN_V26 | GPIO Connection 1[30] |
| GPIO_1[31] | PIN_V25 | GPIO Connection 1[31] |
| GPIO_1[32] | PIN_V24 | GPIO Connection 1[32] |
| GPIO_1[33] | PIN_V23 | GPIO Connection 1[33] |
| GPIO_1[34] | PIN_W25 | GPIO Connection 1[34] |
| GPIO_1[35] | PIN_W23 | GPIO Connection 1[35] |

| HEX3[5] | PIN_U22 | Seven Segment Digit 3[5] |
|---|---|---|
| HEX3[6] | PIN_W24 | Seven Segment Digit 3[6] |
| HEX4[0] | PIN_U9 | Seven Segment Digit 4[0] |
| HEX4[1] | PIN_U1 | Seven Segment Digit 4[1] |
| HEX4[2] | PIN_U2 | Seven Segment Digit 4[2] |
| HEX4[3] | PIN_T4 | Seven Segment Digit 4[3] |
| HEX4[4] | PIN_R7 | Seven Segment Digit 4[4] |
| HEX4[5] | PIN_R6 | Seven Segment Digit 4[5] |
| HEX4[6] | PIN_T3 | Seven Segment Digit 4[6] |
| HEX5[0] | PIN_T2 | Seven Segment Digit 5[0] |
| HEX5[1] | PIN_P6 | Seven Segment Digit 5[1] |
| HEX5[2] | PIN_P7 | Seven Segment Digit 5[2] |
| HEX5[3] | PIN_T9 | Seven Segment Digit 5[3] |
| HEX5[4] | PIN_R5 | Seven Segment Digit 5[4] |
| HEX5[5] | PIN_R4 | Seven Segment Digit 5[5] |
| HEX5[6] | PIN_R3 | Seven Segment Digit 5[6] |
| HEX6[0] | PIN_R2 | Seven Segment Digit 6[0] |
| HEX6[1] | PIN_P4 | Seven Segment Digit 6[1] |
| HEX6[2] | PIN_P3 | Seven Segment Digit 6[2] |
| HEX6[3] | PIN_M2 | Seven Segment Digit 6[3] |
| HEX6[4] | PIN_M3 | Seven Segment Digit 6[4] |
| HEX6[5] | PIN_M5 | Seven Segment Digit 6[5] |
| HEX6[6] | PIN_M4 | Seven Segment Digit 6[6] |
| HEX7[0] | PIN_L3 | Seven Segment Digit 7[0] |
| HEX7[1] | PIN_L2 | Seven Segment Digit 7[1] |
| HEX7[2] | PIN_L9 | Seven Segment Digit 7[2] |
| HEX7[3] | PIN_L6 | Seven Segment Digit 7[3] |
| HEX7[4] | PIN_L7 | Seven Segment Digit 7[4] |
| HEX7[5] | PIN_P9 | Seven Segment Digit 7[5] |
| HEX7[6] | PIN_N9 | Seven Segment Digit 7[6] |
| **Signal Name** | **FPGA Pin No.** | **Description** |



# On the “compiler” / “programmer”

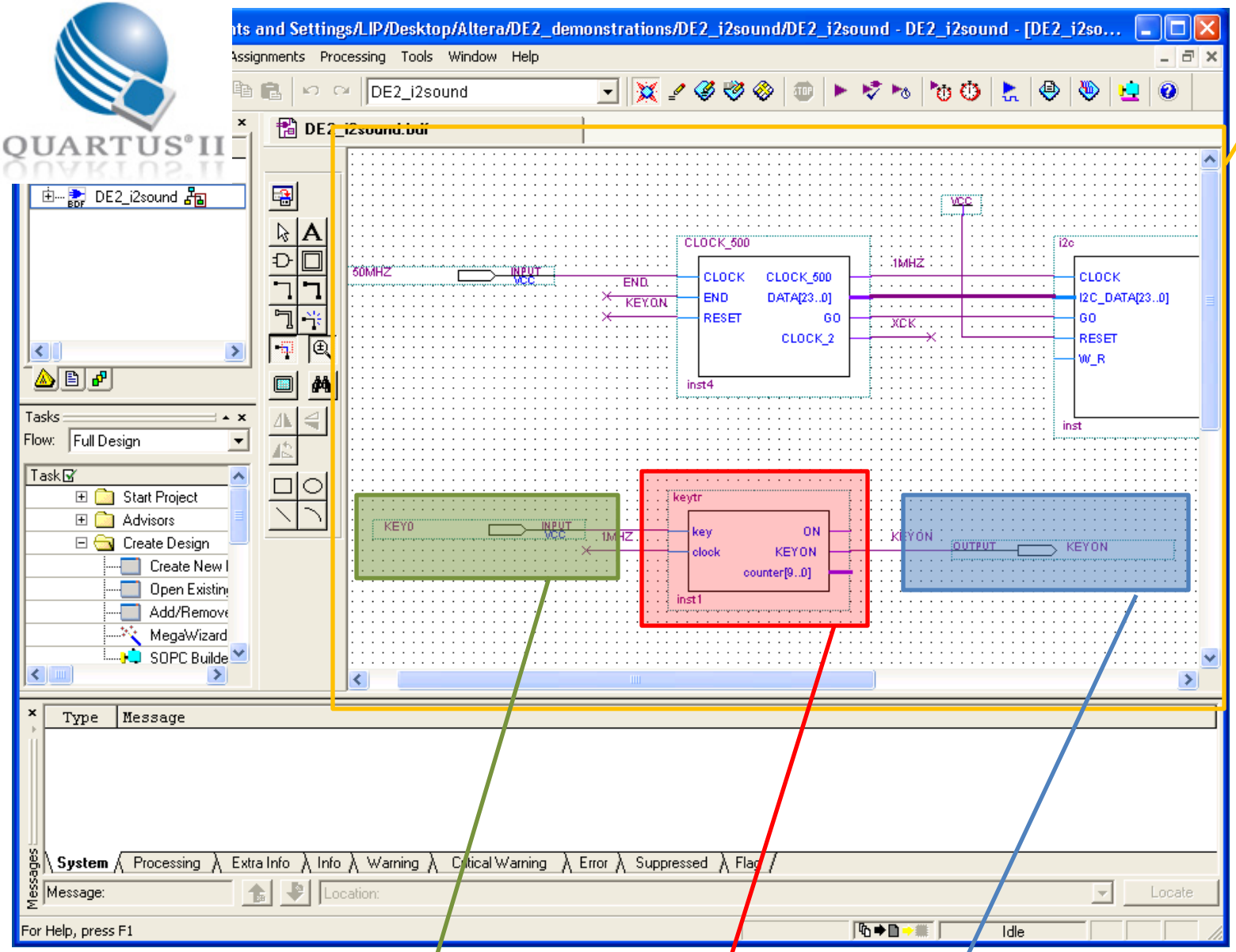



Friendly Name

Physical Names

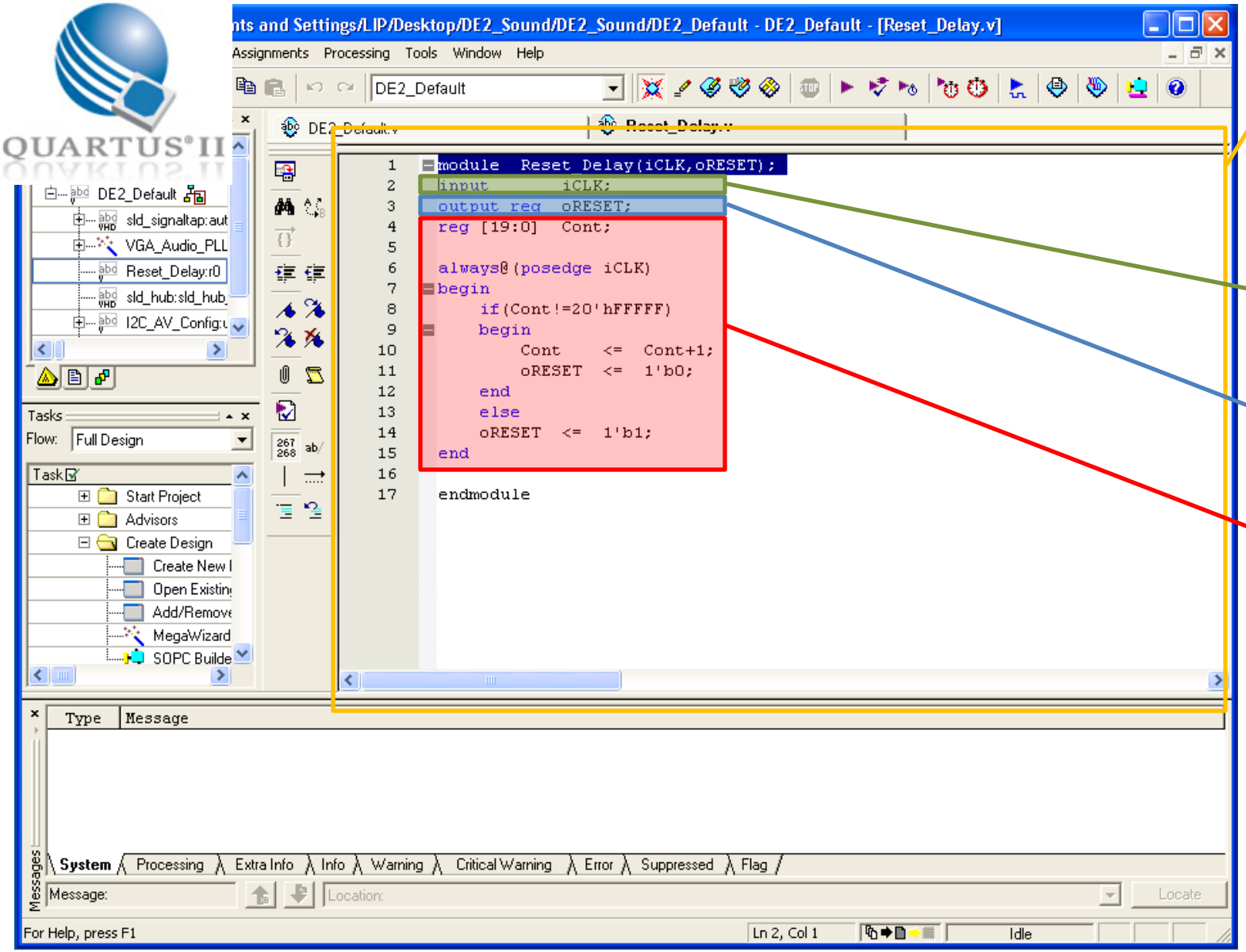
# Software - esquemático

**Programação esquemático**




**Input** **Lógica** **Output**

# Software - verilog




**Programação esquemático**

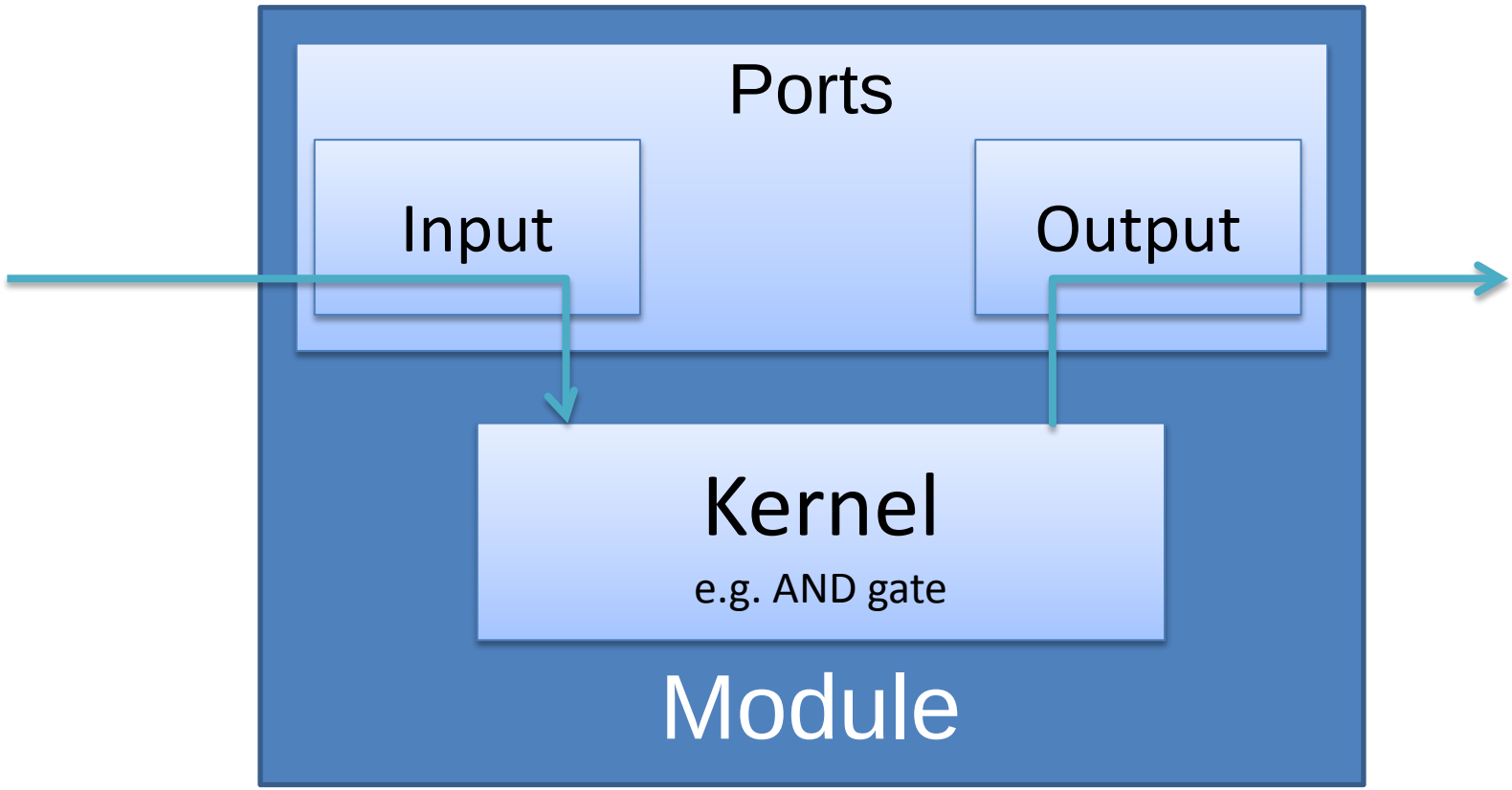
**Input**

**Output**

**Lógica**

# Structuring... Modules

Modules are the building blocks in Verilog!
There is at least one module: The top one that has the name of the project!




Ports in the top level module link directly to the pins

# Now, the text you need to write that the compiler will interpret with the configuration for the FPGA to do what you want.
# a.k.a. code

```
module mux(input a,b,sel, output q, qbar);
   wire selbar, q1, q2;
   not n1(selbar, sel);
   and a1(q1, a, selbar);
   and a2(z2, b, sel);
   or o1(q, q1, q2);
   not n2(qbar, q)
endmodule
```

Selbar, q1, q2 are names given to wires

not, and, or are modules! n1, a1, a2, o1, n2 are names of instances

# Another way...

```
module mux(input a,b,sel, output q, qbar);

   assign q = sel? a : b;
   assign qbar = ~ q;


endmodule
```

Same as
If (sel) then a else b

Assign means that
Left Hand Side (LHS)
of '=' takes 'immediately' the value that results from
Right Hand Side (RHS)

# Yet another way...

```
module mux(input a,b,sel, output reg q, qbar);

   always @ (a,b,sel) begin
     if (sel) q=a;
     else q=b;
   end
   assign qbar = ~ q;

endmodule
```

Notice the **reg** keyword...

"*Whenever a,b or sel changes*"

Can be replaced by
always @ (*)
"*Whenever anything changes*"

If and cases can be used

*Beware of c-like syntax... You are **NOT** programming a microprocessor*

# Verilog data values

| Value | Meaning |
|---|---|
| 0 | Logic zero, “Low” |
| 1 | Logic one, “High” |
| Z or ? | High Impedance (tri-state) |
| X | Unknow (simulation) |

# Numeric constants

Full format: <Width>’<Radix>value
Width: number
Radix: d=decimal, h=hex, o=ocatl, b=binary

| Value | Meaning |
|---|---|
| 123 | Default: decimal radix |
| ‘d123 | ‘d=decimal radix |
| ‘h7B | ‘h=hexadecimal radix |
| ‘o173 | ‘o=ocatl radix |
| ‘b111_101 | ‘b=binary radix |
| 16’b11111 | A binary with 16 bits |
| 16’d5 | A 16 bit decimal = ‘b0000_0000_0000_0101 |

# How many bits?

| | |
|---|---|
| Wire ab; | A 1 bit wire called ab |
| Wire ab,cd; | Two 1 bit wires called ab and cd |
| wire [31:0] ef; | A 32 bits wire bus called ef; |
| {ab,cd} | Concatenation of ab and cd; |
| ef[15] | Bit #15 (the sixteenth) of ef |
| ef[7:0] | First 8 bits of ef (the ones to the right |

## What does this means?

```
wire [31:0] kk;
Wire [7:0] a,b,c,d;
Assign kk={d,c,b,a}
```

# Boolean operators

- Bitwise operators perform bit-oriented operations on vectors
  - ~(4'b0101) = {~0,~1,~0,~1} = 4'b1010
  - 4'b0101 & 4'b0011 = {0&0, 1&0, 0&1, 1&1} = 4'b0001
- Reduction operators act on each bit of a single input vector
  - &(4'b0101) = 0 & 1 & 0 & 1 = 1'b0
- Logical operators return one-bit (true/false) results
  - !(4'b0101) = 1'b0

Bitwise

| | |
|---|---|
| ~a | NOT |
| a & b | AND |
| a \| b | OR |
| a ^ b | XOR |
| a ~^ b<br>a ^~ b | XNOR |

Reduction

| | |
|---|---|
| &a | AND |
| ~&a | NAND |
| \|a | OR |
| ~\|a | NOR |
| ^a | XOR |
| ~^a<br>^~a | XNOR |

*Note distinction between ~a and !a when operating on multi-bit values*

Logical

| | |
|---|---|
| !a | NOT |
| a && b | AND |
| a \|\| b | OR |
| a == b<br>a != b | [in]equality<br>returns x when x or z in bits. Else returns 0 or 1 |
| a === b<br>a !== b | case [in]equality<br>returns 0 or 1 based on bit by bit comparison |

# Other operators

Conditional

| | |
|---|---|
| a ? b : c | If a then b else c |

Relational

| | |
|---|---|
| a > b | greater than |
| a >= b | greater than or equal |
| a < b | Less than |
| a <= b | Less than or equal |

Arithmetic

| | |
|---|---|
| -a | negate |
| a + b | add |
| a - b | subtract |
| a * b | multiply |
| a / b | divide |
| a % b | modulus |
| a ** b | exponentiate |
| a << b | logical left shift |
| a >> b | logical right shift |
| a <<< b | arithmetic left shift |
| a >>> b | arithmetic right shift |

# And now our lab session...

Two simple exercises:

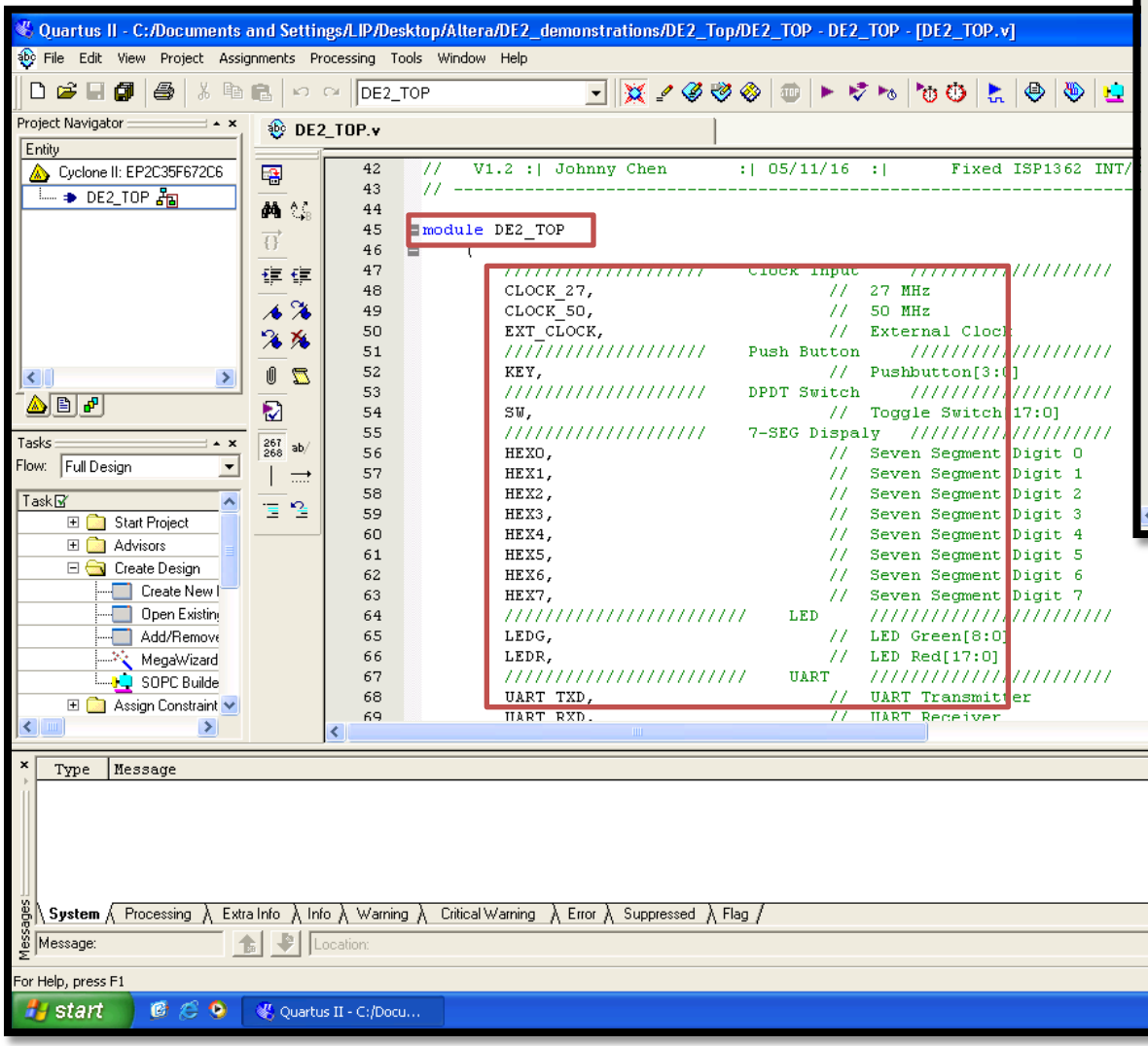
1) “OLA MUNDO” just play dorectly with bits

2) Make a module that has:
   - Inputs: 4 bits codificam numero binario
   - Ouputs: as 7 linhas de 1 display de 7 segmentos
   - kernel: activar segmentos do display para mostrar número

## Helps…

Usign DE2 you get all hardware issues “solved”
DE2_TOP project is a bare project: use it
DE2_TOP already has “friendly names”
DE2_TOP has some assigns... Play with them

# File→Open Project→DE2_top



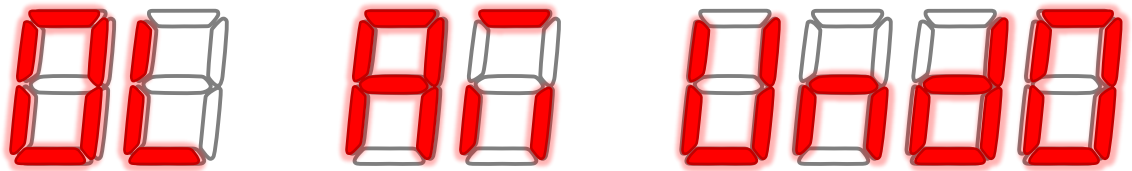

```
//   V1.2 :| Johnny Chen       :| 05/11/16  :|      Fixed ISP1362 INT/
// --------------------------------------------------------------------

module DE2_TOP
(
    ////////////////////    Clock Input     ////////////////////
    CLOCK_27,                       //  27 MHz
    CLOCK_50,                       //  50 MHz
    EXT_CLOCK,                      //  External Clock
    ////////////////////    Push Button     ////////////////////
    KEY,                            //  Pushbutton[3:0]
    ////////////////////    DPDT Switch     ////////////////////
    SW,                             //  Toggle Switch[17:0]
    ////////////////////    7-SEG Dispaly   ////////////////////
    HEX0,                           //  Seven Segment Digit 0
    HEX1,                           //  Seven Segment Digit 1
    HEX2,                           //  Seven Segment Digit 2
    HEX3,                           //  Seven Segment Digit 3
    HEX4,                           //  Seven Segment Digit 4
    HEX5,                           //  Seven Segment Digit 5
    HEX6,                           //  Seven Segment Digit 6
    HEX7,                           //  Seven Segment Digit 7
    ////////////////////////    LED     ////////////////////////
    LEDG,                           //  LED Green[8:0]
    LEDR,                           //  LED Red[17:0]
    ////////////////////////    UART    ////////////////////////
    UART_TXD,                       //  UART Transmitter
    UART_RXD,                       //  UART Receiver
```

```
////////////////////////    Clock Input     ////////////////////////
input           CLOCK_27;               //  27 MHz
input           CLOCK_50;               //  50 MHz
input           EXT_CLOCK;              //  External Clock
////////////////////////    Push Button     ////////////////////////
input   [3:0]   KEY;                    //  Pushbutton[3:0]
////////////////////////    DPDT Switch     ////////////////////////
input   [17:0]  SW;                     //  Toggle Switch[17:0]
////////////////////////    7-SEG Dispaly   ////////////////////////
output  [6:0]   HEX0;                   //  Seven Segment Digit 0
output  [6:0]   HEX1;                   //  Seven Segment Digit 1
output  [6:0]   HEX2;                   //  Seven Segment Digit 2
output  [6:0]   HEX3;                   //  Seven Segment Digit 3
output  [6:0]   HEX4;                   //  Seven Segment Digit 4
output  [6:0]   HEX5;                   //  Seven Segment Digit 5
output  [6:0]   HEX6;                   //  Seven Segment Digit 6
output  [6:0]   HEX7;                   //  Seven Segment Digit 7
////////////////////////////    LED     ////////////////////////////
output  [8:0]   LEDG;                   //  LED Green[8:0]
output  [17:0]  LEDR;                   //  LED Red[17:0]
////////////////////////////    UART    ////////////////////////////
output          UART_TXD;               //  UART Transmitter
input           UART_RXD;               //  UART Receiver
////////////////////////////    IRDA    ////////////////////////////
output          IRDA_TXD;               //  IRDA Transmitter
input           IRDA_RXD;               //  IRDA Receiver
////////////////////////    SDRAM Interface ////////////////////////
inout   [15:0]  DRAM_DQ;                //  SDRAM Data bus 16 Bits
output  [11:0]  DRAM_ADDR;              //  SDRAM Address bus 12 Bits
```

```
//  Turn on all display
assign  HEX0        =   7'h00;
assign  HEX1        =   7'h00;
assign  HEX2        =   7'h00;
assign  HEX3        =   7'h00;
assign  HEX4        =   7'h00;
assign  HEX5        =   7'h00;
assign  HEX6        =   7'h00;
assign  HEX7        =   7'h00;
assign  LEDG    =   9'h1FF;
assign  LEDR        =   18'h3FFFF;
assign  LCD_ON      =   1'b1;
assign  LCD_BLON    =   1'b1;

//  All inout port turn to tri-state
assign  DRAM_DQ     =   16'hzzzz;
assign  FL_DQ       =   8'hzz;
assign  SRAM_DQ     =   16'hzzzz;
assign  OTG_DATA    =   16'hzzzz;
assign  LCD_DATA    =   8'hzz;
assign  SD_DAT      =   1'bz;
assign  I2C_SDAT    =   1'bz;
assign  ENET_DATA   =   16'hzzzz;
assign  AUD_ADCLRCK =   1'bz;
assign  AUD_DACLRCK =   1'bz;
assign  AUD_BCLK    =   1'bz;
assign  GPIO_0      =   36'hzzzzzzzzz;
assign  GPIO_1      =   36'hzzzzzzzzz;
```




STOP