

Refs:

Cyclone II device Handbook, Altera corp.
Quartus II Handbook , Altera corp.
DE2 documentation
Verilog HDL, S. Palnitkar, Prentice Hall

- Introdução
 - FPGAs
 - Laboratório
 - Verilog
 - Lógica combinatória
 - Lógica sequencial
- Máquinas estado
- Advanced verilog (video, etc.)

Programação de Lógica Digital...

Estrutura

Trabalhos:

Ex1: Ola Mundo

Ex2: Cronómetro

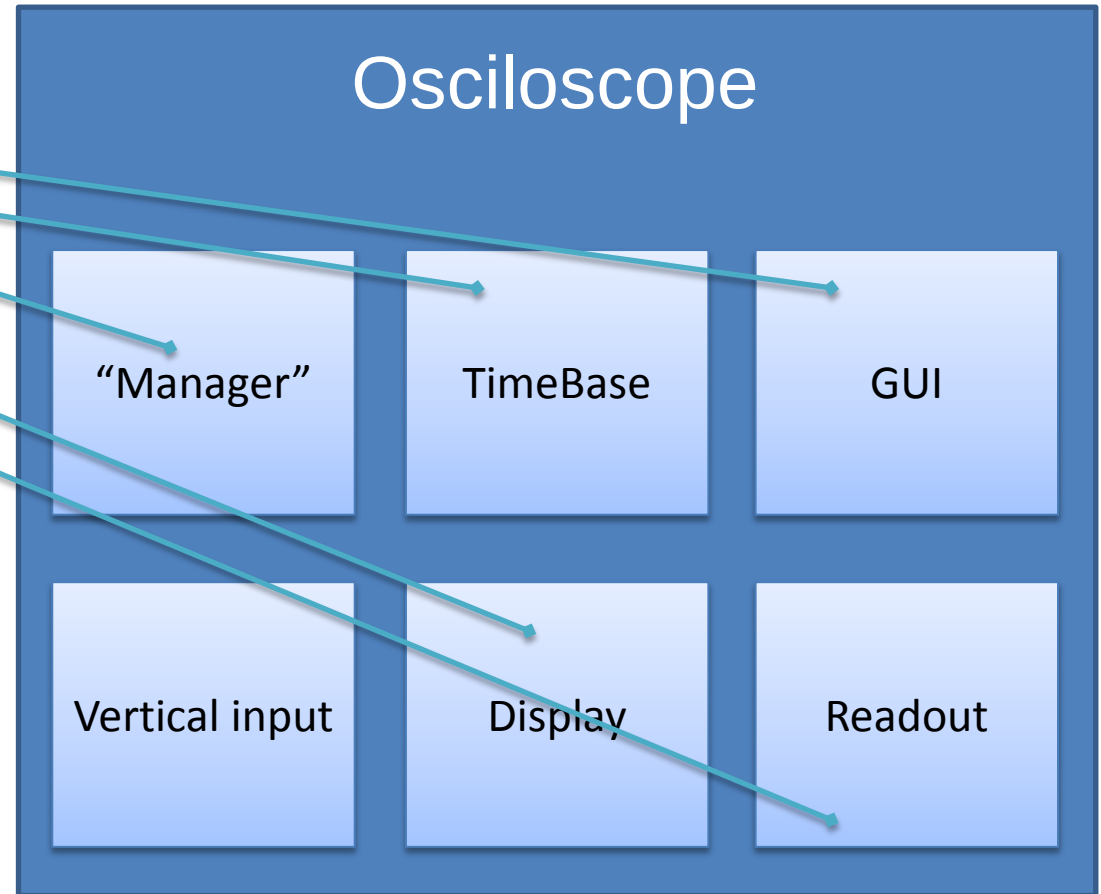
Ex3: Máquinas Estados

Ex4: Mira Técnica

Ex5: Microprocessador

T1: Osciloscópio

T2: à escolha / negociado



Avaliação

Exercícios avaliados em trinário (0,1,2); valem 25%

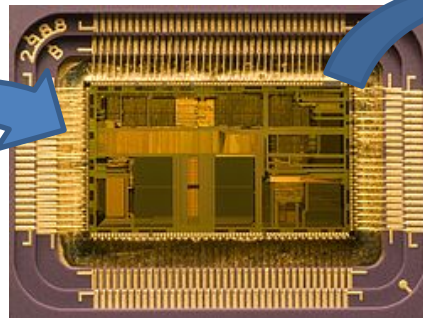
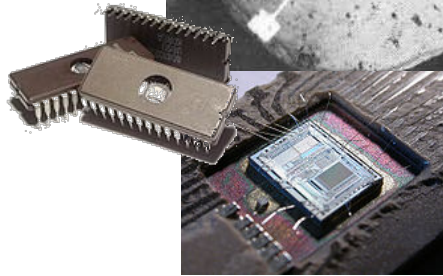
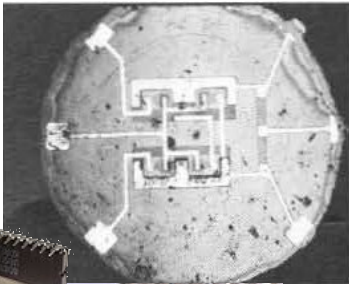
Trabalho 1: Avaliação 0-20; vale 25%

Trabalho2: Avaliação 0-20; vale 50%

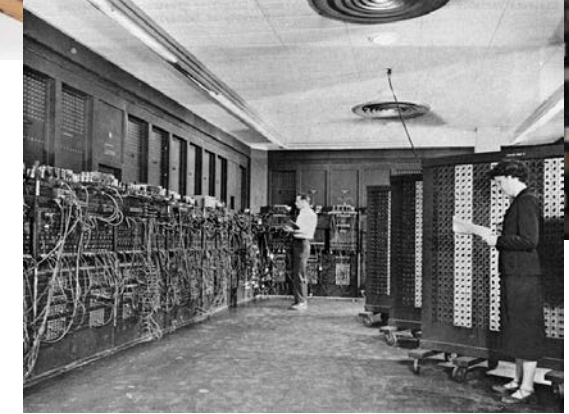
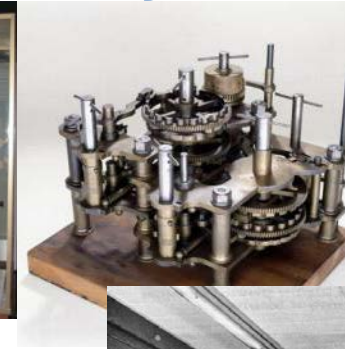
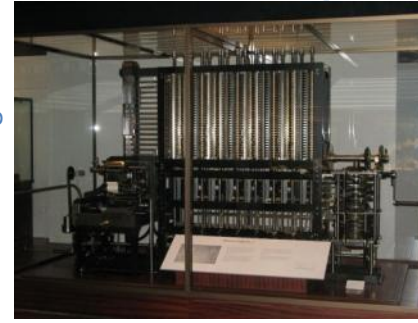
$$\text{Nota} = (\text{Ex1} + \text{Ex2} + \text{Ex3} + \text{Ex4} + \text{Ex5}) / 5 * 10 * 0.25 + \text{T1} * 0.25 + \text{T2} * 0.5$$

Lógica Digital

Programação



Babbage
difference engine



Lógica Digital de Programação

Tudo funciona ou por magia ou com gnomos...

Programação de microprocessadores (assembly, c++, etc.)

Dar ao “gnomo” uma lista
(consecutiva) de operações a
realizar

1 Máquina executa várias tarefas
consecutivas



Programação de Lógica Digital (FPGAs+HDL)

Dar ao gnomo uma lista de
“objectos” para construir

Várias Máquinas executam várias
tarefas em paralelo



Em linguagens de alto nível por vezes confundem-se



2+2?
Resultado x 2?

A=2+2
Cout << A
A=A*2
Cout << A

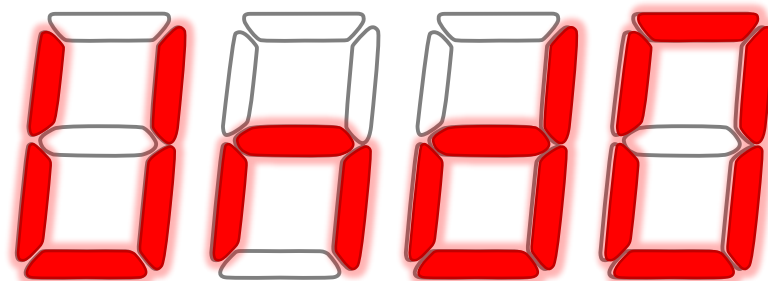
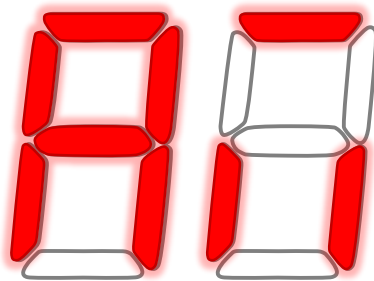
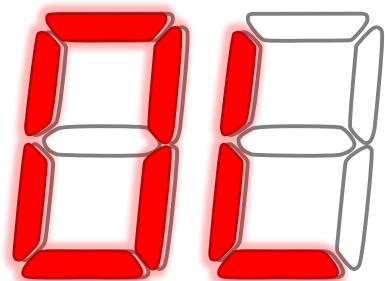
A=4
4!
A=8
8!

tempo

A=2+2
Output A
A=A*2
Output A

Somador: A=4
“ao mesmo tempo”
Multiplicador: A=A*2
Saída ??? (glitches?)

Uma FPGA a funcionar...



Primeiro exercício...

Hardware

DLA7Uhd0



OLA!Undo



DE2_Pin Table.pdf

Altera DE2 Board Pin Table		
Signal Name	PPGA Pin No.	Description
SW[0]	PNL_A05	Toggle Switch[0]
SW[1]	PNL_A06	Toggle Switch[1]
SW[2]	PNL_P20	Toggle Switch[2]
SW[3]	PNL_A04	Toggle Switch[3]
SW[4]	PNL_A07	Toggle Switch[4]
SW[5]	PNL_A08	Toggle Switch[5]
SW[6]	PNL_A09	Toggle Switch[6]
SW[7]	PNL_C10	Toggle Switch[7]
SW[8]	PNL_B13	Toggle Switch[8]
SW[9]	PNL_A13	Toggle Switch[9]
SW[10]	PNL_P01	Toggle Switch[10]
SW[11]	PNL_P02	Toggle Switch[11]
SW[12]	PNL_P03	Toggle Switch[12]
SW[13]	PNL_P04	Toggle Switch[13]
SW[14]	PNL_P05	Toggle Switch[14]
SW[15]	PNL_P06	Toggle Switch[15]
SW[16]	PNL_P07	Toggle Switch[16]
SW[17]	PNL_P08	Toggle Switch[17]
Signal Name	PPGA Pin No.	Description
DRAM_A0[0:3]	PNL_P16	SDRAM Address[0]
DRAM_A0[4:7]	PNL_P17	SDRAM Address[4]
DRAM_A0[8:11]	PNL_P18	SDRAM Address[8]
DRAM_A0[12:15]	PNL_P19	SDRAM Address[12]
DRAM_A0[16:19]	PNL_P20	SDRAM Address[16]
DRAM_A0[20:23]	PNL_P21	SDRAM Address[20]
DRAM_A0[24:27]	PNL_P22	SDRAM Address[24]
DRAM_A0[28:31]	PNL_P23	SDRAM Address[28]
DRAM_A0[32:35]	PNL_P24	SDRAM Address[32]
DRAM_A0[36:39]	PNL_P25	SDRAM Address[36]
DRAM_A0[40:43]	PNL_P26	SDRAM Address[40]
DRAM_A0[44:47]	PNL_P27	SDRAM Address[44]
DRAM_A0[48:51]	PNL_P28	SDRAM Address[48]
DRAM_A0[52:55]	PNL_P29	SDRAM Address[52]
DRAM_A0[56:59]	PNL_P30	SDRAM Address[56]
DRAM_A0[60:63]	PNL_P31	SDRAM Address[60]
DRAM_A0[64:67]	PNL_P32	SDRAM Address[64]
DRAM_A0[68:71]	PNL_P33	SDRAM Address[68]
DRAM_A0[72:75]	PNL_P34	SDRAM Address[72]
DRAM_A0[76:79]	PNL_P35	SDRAM Address[76]
DRAM_A0[80:83]	PNL_P36	SDRAM Address[80]
DRAM_A0[84:87]	PNL_P37	SDRAM Address[84]
DRAM_A0[88:91]	PNL_P38	SDRAM Address[88]
DRAM_A0[92:95]	PNL_P39	SDRAM Address[92]
DRAM_A0[96:99]	PNL_P40	SDRAM Address[96]
DRAM_A0[100:103]	PNL_P41	SDRAM Address[100]
DRAM_A0[104:107]	PNL_P42	SDRAM Address[104]
DRAM_A0[108:111]	PNL_P43	SDRAM Address[108]
DRAM_A0[112:115]	PNL_P44	SDRAM Address[112]
DRAM_A0[116:119]	PNL_P45	SDRAM Address[116]
DRAM_A0[120:123]	PNL_P46	SDRAM Address[120]
DRAM_A0[124:127]	PNL_P47	SDRAM Address[124]
DRAM_A0[128:131]	PNL_P48	SDRAM Address[128]
DRAM_A0[132:135]	PNL_P49	SDRAM Address[132]
DRAM_A0[136:139]	PNL_P50	SDRAM Address[136]
DRAM_A0[140:143]	PNL_P51	SDRAM Address[140]
DRAM_A0[144:147]	PNL_P52	SDRAM Address[144]
DRAM_A0[148:151]	PNL_P53	SDRAM Address[148]
DRAM_A0[152:155]	PNL_P54	SDRAM Address[152]
DRAM_A0[156:159]	PNL_P55	SDRAM Address[156]
DRAM_A0[160:163]	PNL_P56	SDRAM Address[160]
DRAM_A0[164:167]	PNL_P57	SDRAM Address[164]
DRAM_A0[168:171]	PNL_P58	SDRAM Address[168]
DRAM_A0[172:175]	PNL_P59	SDRAM Address[172]
DRAM_A0[176:179]	PNL_P60	SDRAM Address[176]
DRAM_A0[180:183]	PNL_P61	SDRAM Address[180]
DRAM_A0[184:187]	PNL_P62	SDRAM Address[184]
DRAM_A0[188:191]	PNL_P63	SDRAM Address[188]
DRAM_A0[192:195]	PNL_P64	SDRAM Address[192]
DRAM_A0[196:199]	PNL_P65	SDRAM Address[196]
DRAM_A0[200:203]	PNL_P66	SDRAM Address[200]
DRAM_A0[204:207]	PNL_P67	SDRAM Address[204]
DRAM_A0[208:211]	PNL_P68	SDRAM Address[208]
DRAM_A0[212:215]	PNL_P69	SDRAM Address[212]
DRAM_A0[216:219]	PNL_P70	SDRAM Address[216]
DRAM_A0[220:223]	PNL_P71	SDRAM Address[220]
DRAM_A0[224:227]	PNL_P72	SDRAM Address[224]
DRAM_A0[228:231]	PNL_P73	SDRAM Address[228]
DRAM_A0[232:235]	PNL_P74	SDRAM Address[232]
DRAM_A0[236:239]	PNL_P75	SDRAM Address[236]
DRAM_A0[240:243]	PNL_P76	SDRAM Address[240]
DRAM_A0[244:247]	PNL_P77	SDRAM Address[244]
DRAM_A0[248:251]	PNL_P78	SDRAM Address[248]
DRAM_A0[252:255]	PNL_P79	SDRAM Address[252]
DRAM_A0[256:259]	PNL_P80	SDRAM Address[256]
DRAM_A0[260:263]	PNL_P81	SDRAM Address[260]
DRAM_A0[264:267]	PNL_P82	SDRAM Address[264]
DRAM_A0[268:271]	PNL_P83	SDRAM Address[268]
DRAM_A0[272:275]	PNL_P84	SDRAM Address[272]
DRAM_A0[276:279]	PNL_P85	SDRAM Address[276]
DRAM_A0[280:283]	PNL_P86	SDRAM Address[280]
DRAM_A0[284:287]	PNL_P87	SDRAM Address[284]
DRAM_A0[288:291]	PNL_P88	SDRAM Address[288]
DRAM_A0[292:295]	PNL_P89	SDRAM Address[292]
DRAM_A0[296:299]	PNL_P90	SDRAM Address[296]
DRAM_A0[300:303]	PNL_P91	SDRAM Address[300]
DRAM_A0[304:307]	PNL_P92	SDRAM Address[304]
DRAM_A0[308:311]	PNL_P93	SDRAM Address[308]
DRAM_A0[312:315]	PNL_P94	SDRAM Address[312]
DRAM_A0[316:319]	PNL_P95	SDRAM Address[316]
DRAM_A0[320:323]	PNL_P96	SDRAM Address[320]
DRAM_A0[324:327]	PNL_P97	SDRAM Address[324]
DRAM_A0[328:331]	PNL_P98	SDRAM Address[328]
DRAM_A0[332:335]	PNL_P99	SDRAM Address[332]
DRAM_A0[336:339]	PNL_P100	SDRAM Address[336]
DRAM_A0[340:343]	PNL_P101	SDRAM Address[340]
DRAM_A0[344:347]	PNL_P102	SDRAM Address[344]
DRAM_A0[348:351]	PNL_P103	SDRAM Address[348]
DRAM_A0[352:355]	PNL_P104	SDRAM Address[352]
DRAM_A0[356:359]	PNL_P105	SDRAM Address[356]
DRAM_A0[360:363]	PNL_P106	SDRAM Address[360]
DRAM_A0[364:367]	PNL_P107	SDRAM Address[364]
DRAM_A0[368:371]	PNL_P108	SDRAM Address[368]
DRAM_A0[372:375]	PNL_P109	SDRAM Address[372]
DRAM_A0[376:379]	PNL_P110	SDRAM Address[376]
DRAM_A0[380:383]	PNL_P111	SDRAM Address[380]
DRAM_A0[384:387]	PNL_P112	SDRAM Address[384]
DRAM_A0[388:391]	PNL_P113	SDRAM Address[388]
DRAM_A0[392:395]	PNL_P114	SDRAM Address[392]
DRAM_A0[396:399]	PNL_P115	SDRAM Address[396]
DRAM_A0[400:403]	PNL_P116	SDRAM Address[400]
DRAM_A0[404:407]	PNL_P117	SDRAM Address[404]
DRAM_A0[408:411]	PNL_P118	SDRAM Address[408]
DRAM_A0[412:415]	PNL_P119	SDRAM Address[412]
DRAM_A0[416:419]	PNL_P120	SDRAM Address[416]
DRAM_A0[420:423]	PNL_P121	SDRAM Address[420]
DRAM_A0[424:427]	PNL_P122	SDRAM Address[424]
DRAM_A0[428:431]	PNL_P123	SDRAM Address[428]
DRAM_A0[432:435]	PNL_P124	SDRAM Address[432]
DRAM_A0[436:439]	PNL_P125	SDRAM Address[436]
DRAM_A0[440:443]	PNL_P126	SDRAM Address[440]
DRAM_A0[444:447]	PNL_P127	SDRAM Address[444]
DRAM_A0[448:451]	PNL_P128	SDRAM Address[448]
DRAM_A0[452:455]	PNL_P129	SDRAM Address[452]
DRAM_A0[456:459]	PNL_P130	SDRAM Address[456]
DRAM_A0[460:463]	PNL_P131	SDRAM Address[460]
DRAM_A0[464:467]	PNL_P132	SDRAM Address[464]
DRAM_A0[468:471]	PNL_P133	SDRAM Address[468]
DRAM_A0[472:475]	PNL_P134	SDRAM Address[472]
DRAM_A0[476:479]	PNL_P135	SDRAM Address[476]
DRAM_A0[480:483]	PNL_P136	SDRAM Address[480]
DRAM_A0[484:487]	PNL_P137	SDRAM Address[484]
DRAM_A0[488:491]	PNL_P138	SDRAM Address[488]
DRAM_A0[492:495]	PNL_P139	SDRAM Address[492]
DRAM_A0[496:499]	PNL_P140	SDRAM Address[496]
DRAM_A0[500:503]	PNL_P141	SDRAM Address[500]
DRAM_A0[504:507]	PNL_P142	SDRAM Address[504]
DRAM_A0[508:511]	PNL_P143	SDRAM Address[508]
DRAM_A0[512:515]	PNL_P144	SDRAM Address[512]
DRAM_A0[516:519]	PNL_P145	SDRAM Address[516]
DRAM_A0[520:523]	PNL_P146	SDRAM Address[520]
DRAM_A0[524:527]	PNL_P147	SDRAM Address[524]
DRAM_A0[528:531]	PNL_P148	SDRAM Address[528]
DRAM_A0[532:535]	PNL_P149	SDRAM Address[532]
DRAM_A0[536:539]	PNL_P150	SDRAM Address[536]
DRAM_A0[540:543]	PNL_P151	SDRAM Address[540]
DRAM_A0[544:547]	PNL_P152	SDRAM Address[544]
DRAM_A0[548:551]	PNL_P153	SDRAM Address[548]
DRAM_A0[552:555]	PNL_P154	SDRAM Address[552]
DRAM_A0[556:559]	PNL_P155	SDRAM Address[556]
DRAM_A0[560:563]	PNL_P156	SDRAM Address[560]
DRAM_A0[564:567]	PNL_P157	SDRAM Address[564]
DRAM_A0[568:571]	PNL_P158	SDRAM Address[568]
DRAM_A0[572:575]	PNL_P159	SDRAM Address[572]
DRAM_A0[576:579]	PNL_P160	SDRAM Address[576]
DRAM_A0[580:583]	PNL_P161	SDRAM Address[580]
DRAM_A0[584:587]	PNL_P162	SDRAM Address[584]
DRAM_A0[588:591]	PNL_P163	SDRAM Address[588]
DRAM_A0[592:595]	PNL_P164	SDRAM Address[592]
DRAM_A0[596:599]	PNL_P165	SDRAM Address[596]
DRAM_A0[600:603]	PNL_P166	SDRAM Address[600]
DRAM_A0[604:607]	PNL_P167	SDRAM Address[604]
DRAM_A0[608:611]	PNL_P168	SDRAM Address[608]
DRAM_A0[612:615]	PNL_P169	SDRAM Address[612]
DRAM_A0[616:619]	PNL_P170	SDRAM Address[616]
DRAM_A0[620:623]	PNL_P171	SDRAM Address[620]
DRAM_A0[624:627]	PNL_P172	SDRAM Address[624]
DRAM_A0[628:631]	PNL_P173	SDRAM Address[628]
DRAM_A0[632:635]	PNL_P174	SDRAM Address[632]
DRAM_A0[636:639]	PNL_P175	SDRAM Address[636]
DRAM_A0[640:643]	PNL_P176	SDRAM Address[640]
DRAM_A0[644:647]	PNL_P177	SDRAM Address[644]
DRAM_A0[648:651]	PNL_P178	SDRAM Address[648]
DRAM_A0[652:655]	PNL_P179	SDRAM Address[652]
DRAM_A0[656:659]	PNL_P180	SDRAM Address[656]
DRAM_A0[660:663]	PNL_P181	SDRAM Address[660]
DRAM_A0[664:667]	PNL_P182	SDRAM Address[664]
DRAM_A0[668:671]	PNL_P183	SDRAM Address[668]
DRAM_A0[672:675]	PNL_P184	SDRAM Address[672]
DRAM_A0[676:679]	PNL_P185	SDRAM Address[676]
DRAM_A0[680:683]	PNL_P186	SDRAM Address[680]
DRAM_A0[684:687]	PNL_P187	SDRAM Address[684]
DRAM_A0[688:691]	PNL_P188	SDRAM Address[688]
DRAM_A0[692:695]	PNL_P189	SDRAM Address[692]
DRAM_A0[696:699]	PNL_P190	SDRAM Address[696]
DRAM_A0[700:703]	PNL_P191	SDRAM Address[700]
DRAM_A0[704:707]	PNL_P192	SDRAM Address[704]
DRAM_A0[708:711]	PNL_P193	SDRAM Address[708]
DRAM_A0[712:715]	PNL_P194	SDRAM Address[712]
DRAM_A0[716:719]	PNL_P195	SDRAM Address[716]
DRAM_A0[720:723]	PNL_P196	SDRAM Address[720]
DRAM_A0[724:727]	PNL_P197	SDRAM Address[724]
DRAM_A0[728:731]	PNL_P198	SDRAM Address[728]
DRAM_A0[732:735]	PNL_P199	SDRAM Address[732]
DRAM_A0[736:739]	PNL_P200	SDRAM Address[736]
DRAM_A0[740:743]	PNL_P201	SDRAM Address[740]
DRAM_A0[744:747]	PNL_P202	SDRAM Address[744]
DRAM_A0[748:751]	PNL_P203	SDRAM Address[748]
DRAM_A0[752:755]	PNL_P204	SDRAM Address[752]
DRAM_A0[756:759]	PNL_P205	SDRAM Address[756]
DRAM_A0[760:763]	PNL_P206	SDRAM Address[760]
DRAM_A0[764:767]	PNL_P207	SDRAM Address[764]
DRAM_A0[768:771]	PNL_P208	SDRAM Address[768]
DRAM_A0[772:775]	PNL_P209	SDRAM Address[772]
DRAM_A0[776:779]	PNL_P210	SDRAM Address[776]
DRAM_A0[780:783]	PNL_P211	SDRAM Address[780]
DRAM_A0[784:787]	PNL_P212	SDRAM Address[784]
DRAM_A0[788:791]	PNL_P213	SDRAM Address[788]
DRAM_A0[792:795]	PNL_P214	SDRAM Address[792]
DRAM_A0[796:799]	PNL_P215	SDRAM Address[796]
DRAM_A0[800:803]	PNL_P216	SDRAM Address[800]
DRAM_A0[804:807]	PNL_P217	SDRAM Address[804]
DRAM_A0[808:811]	PNL_P218	SDRAM Address[808]
DRAM_A0[812:815]	PNL_P219	SDRAM Address[812]
DRAM_A0[816:819]	PNL_P220	SDRAM Address[816]
DRAM_A0[820:823]	PNL_P221	SDRAM Address[820]
DRAM_A0[824:827]	PNL_P222	SDRAM Address[824]
DRAM_A0[828:831]	PNL_P223	SDRAM Address[828]
DRAM_A0[832:835]	PNL_P224	SDRAM Address[832]
DRAM_A0[836:839]	PNL_P225	SDRAM Address[836]
DRAM_A0[840:843]	PNL_P226	SDRAM Address[840]
DRAM_A0[844:847]	PNL_P227	SDRAM Address[844]
DRAM_A0[848:851]	PNL_P228	SDRAM Address[848]
DRAM_A0[852:855]	PNL_P229	SDRAM Address[852]
DRAM_A0[856:859]	PNL_P230	SDRAM Address[856]
DRAM_A0[860:863]	PNL_P231	SDRAM Address[860]
DRAM_A0[864:867]	PNL_P232	SDRAM Address[864]
DRAM_A0[868:871]	PNL_P233	SDRAM Address[868]
DRAM_A0[872:875]	PNL_P234	SDRAM Address[872]
DRAM_A0[876:879]	PNL_P235	SDRAM Address[876]
DRAM_A0[880:883]	PNL_P236	SDRAM Address[880]
DRAM_A0[884:887]	PNL_P237	SDRAM Address[884]
DRAM_A0[888:891]	PNL_P238	SDRAM Address[888]
DRAM_A0[892:895]	PNL_P239	SDRAM Address[892]
DRAM_A0[896:899]	PNL_P240	SDRAM Address[896]
DRAM_A0[900:903]	PNL_P241	SDRAM Address[900]
DRAM_A0[904:907]	PNL_P242	SDRAM Address[904]
DRAM_A0[908:911]	PNL_P243	SDRAM Address[908]
DRAM_A0[912:915]	PNL_P244	SDRAM Address[912]
DRAM_A0[916:919]	PNL_P245	SDRAM Address[916]
DRAM_A0[920:923]	PNL_P246	SDRAM Address[920]
DRAM_A0[924:927]	PNL_P247	SDRAM Address[924]
DRAM_A0[928:931]	PNL_P248	SDRAM Address[928]
DRAM_A0[932:935]	PNL_P249	SDRAM Address[932]
DRAM_A0[936:939]	PNL_P250	SDRAM Address[936]
DRAM_A0[940:943]	PNL_P251	SDRAM Address[940]
DRAM_A0[944:947]	PNL_P252	SDRAM Address[944]
DRAM_A0[948:951]	PNL_P253	SDRAM Address[948]
DRAM_A0[952:955]	PNL_P254	SDRAM Address[952]
DRAM_A0[956:959]	PNL_P255	SDRAM Address[956]
DRAM_A0[960:963]	PNL_P256	SDRAM Address[960]
DRAM_A0[964:967]	PNL_P257	SDRAM Address[964]
DRAM_A0[968:971]	PNL_P258	SDRAM Address[968]
DRAM_A0[972:975]	PNL_P259	SDRAM Address[972]
DRAM_A0[976:979]	PNL_P260	SDRAM Address[976]
DRAM_A0[980:983]	PNL_P261	SDRAM Address[980]
DRAM_A0[984:987]	PNL_P262	SDRAM Address[984]
DRAM_A0[988:991]	PNL_P263	SDRAM Address[988]
DRAM_A0[992:995]	PNL_P264	SDRAM Address[992]
DRAM_A0[996:999]	PNL_P265	SDRAM Address[996]

Altera DE2 Board Pin Table		
FL_ADDR0[0]	PP1_A0	FLASH Address[0]
FL_ADDR0[1]	PP1_A1	FLASH Address[1]
FL_ADDR0[2]	PP1_A2	FLASH Address[2]
FL_ADDR0[3]	PP1_A3	FLASH Address[3]
FL_ADDR0[4]	PP1_A4	FLASH Address[4]
FL_ADDR0[5]	PP1_A5	FLASH Address[5]
FL_ADDR0[6]	PP1_A6	FLASH Address[6]
FL_ADDR0[7]	PP1_A7	FLASH Address[7]
FL_ADDR0[8]	PP1_A8	FLASH Address[8]
FL_ADDR0[9]	PP1_A9	FLASH Address[9]
FL_ADDR0[10]	PP1_A10	FLASH Address[10]
FL_ADDR0[11]	PP1_A11	FLASH Address[11]
FL_ADDR0[12]	PP1_A12	FLASH Address[12]
FL_ADDR0[13]	PP1_A13	FLASH Address[13]
FL_ADDR0[14]	PP1_A14	FLASH Address[14]
FL_ADDR0[15]	PP1_A15	FLASH Address[15]
FL_ADDR0[16]	PP1_A16	FLASH Address[16]
FL_ADDR0[17]	PP1_A17	FLASH Address[17]
FL_ADDR0[18]	PP1_A18	FLASH Address[18]
FL_ADDR0[19]	PP1_A19	FLASH Address[19]
FL_ADDR0[20]	PP1_A20	FLASH Address[20]
FL_ADDR0[21]	PP1_A21	FLASH Address[21]
FL_ADDR0[22]	PP1_A22	FLASH Address[22]
FL_ADDR0[23]	PP1_A23	FLASH Address[23]
FL_ADDR0[24]	PP1_A24	FLASH Address[24]
FL_ADDR0[25]	PP1_A25	FLASH Address[25]
FL_ADDR0[26]	PP1_A26	FLASH Address[26]
FL_ADDR0[27]	PP1_A27	FLASH Address[27]
FL_ADDR0[28]	PP1_A28	FLASH Address[28]
FL_ADDR0[29]	PP1_A29	FLASH Address[29]
FL_ADDR0[30]	PP1_A30	FLASH Address[30]
FL_ADDR0[31]	PP1_A31	FLASH Address[31]
FL_ADDR0[32]	PP1_A32	FLASH Address[32]
FL_ADDR0[33]	PP1_A33	FLASH Address[33]
FL_ADDR0[34]	PP1_A34	FLASH Address[34]
FL_ADDR0[35]	PP1_A35	FLASH Address[35]
FL_ADDR0[36]	PP1_A36	FLASH Address[36]
FL_ADDR0[37]	PP1_A37	FLASH Address[37]
FL_ADDR0[38]	PP1_A38	FLASH Address[38]
FL_ADDR0[39]	PP1_A39	FLASH Address[39]
FL_ADDR0[40]	PP1_A40	FLASH Address[40]
FL_ADDR0[41]	PP1_A41	FLASH Address[41]
FL_ADDR0[42]	PP1_A42	FLASH Address[42]
FL_ADDR0[43]	PP1_A43	FLASH Address[43]
FL_ADDR0[44]	PP1_A44	FLASH Address[44]
FL_ADDR0[45]	PP1_A45	FLASH Address[45]
FL_ADDR0[46]	PP1_A46	FLASH Address[46]
FL_ADDR0[47]	PP1_A47	FLASH Address[47]
FL_ADDR0[48]	PP1_A48	FLASH Address[48]
FL_ADDR0[49]	PP1_A49	FLASH Address[49]
FL_ADDR0[50]	PP1_A50	FLASH Address[50]
FL_ADDR0[51]	PP1_A51	FLASH Address[51]
FL_ADDR0[52]	PP1_A52	FLASH Address[52]
FL_ADDR0[53]	PP1_A53	FLASH Address[53]
FL_ADDR0[54]	PP1_A54	FLASH Address[54]
FL_ADDR0[55]	PP1_A55	FLASH Address[55]
FL_ADDR0[56]	PP1_A56	FLASH Address[56]
FL_ADDR0[57]	PP1_A57	FLASH Address[57]
FL_ADDR0[58]	PP1_A58	FLASH Address[58]
FL_ADDR0[59]	PP1_A59	FLASH Address[59]
FL_ADDR0[60]	PP1_A60	FLASH Address[60]
FL_ADDR0[61]	PP1_A61	FLASH Address[61]
FL_ADDR0[62]	PP1_A62	FLASH Address[62]
FL_ADDR0[63]	PP1_A63	FLASH Address[63]
FL_ADDR0[64]	PP1_A64	FLASH Address[64]
FL_ADDR0[65]	PP1_A65	FLASH Address[65]
FL_ADDR0[66]	PP1_A66	FLASH Address[66]
FL_ADDR0[67]	PP1_A67	FLASH Address[67]
FL_ADDR0[68]	PP1_A68	FLASH Address[68]
FL_ADDR0[69]	PP1_A69	FLASH Address[69]
FL_ADDR0[70]	PP1_A70	FLASH Address[70]
FL_ADDR0[71]	PP1_A71	FLASH Address[71]
FL_ADDR0[72]	PP1_A72	FLASH Address[72]
FL_ADDR0[73]	PP1_A73	FLASH Address[73]
FL_ADDR0[74]	PP1_A74	FLASH Address[74]
FL_ADDR0[75]	PP1_A75	FLASH Address[75]
FL_ADDR0[76]	PP1_A76	FLASH Address[76]
FL_ADDR0[77]	PP1_A77	FLASH Address[77]
FL_ADDR0[78]	PP1_A78	FLASH Address[78]
FL_ADDR0[79]	PP1_A79	FLASH Address[79]
FL_ADDR0[80]	PP1_A80	FLASH Address[80]
FL_ADDR0[81]	PP1_A81	FLASH Address[81]
FL_ADDR0[82]	PP1_A82	FLASH Address[82]
FL_ADDR0[83]	PP1_A83	FLASH Address[83]
FL_ADDR0[84]	PP1_A84	FLASH Address[84]
FL_ADDR0[85]	PP1_A85	FLASH Address[85]
FL_ADDR0[86]	PP1_A86	FLASH Address[86]
FL_ADDR0[87]	PP1_A87	FLASH Address[87]
FL_ADDR0[88]	PP1_A88	FLASH Address[88]
FL_ADDR0[89]	PP1_A89	FLASH Address[89]
FL_ADDR0[90]	PP1_A90	FLASH Address[90]
FL_ADDR0[91]	PP1_A91	FLASH Address[91]
FL_ADDR0[92]	PP1_A92	FLASH Address[92]
FL_ADDR0[93]	PP1_A93	FLASH Address[93]
FL_ADDR0[94]	PP1_A94	FLASH Address[94]
FL_ADDR0[95]	PP1_A95	FLASH Address[95]
FL_ADDR0[96]	PP1_A96	FLASH Address[96]
FL_ADDR0[97]	PP1_A97	FLASH Address[97]
FL_ADDR0[98]	PP1_A98	FLASH Address[98]
FL_ADDR0[99]	PP1_A99	FLASH Address[99]
FL_ADDR0[100]	PP1_A100	FLASH Address[100]
FL_ADDR0[101]	PP1_A101	FLASH Address[101]
FL_ADDR0[102]	PP1_A102	FLASH Address[102]
FL_ADDR0[103]	PP1_A103	FLASH Address[103]
FL_ADDR0[104]	PP1_A104	FLASH Address[104]
FL_ADDR0[105]	PP1_A105	FLASH Address[105]
FL_ADDR0[106]	PP1_A106	FLASH Address[106]
FL_ADDR0[107]	PP1_A107	FLASH Address[107]
FL_ADDR0[108]	PP1_A108	FLASH Address[108]
FL_ADDR0[109]	PP1_A109	FLASH Address[109]
FL_ADDR0[110]	PP1_A110	FLASH Address[110]
FL_ADDR0[111]	PP1_A111	FLASH Address[111]
FL_ADDR0[112]	PP1_A112	FLASH Address[112]
FL_ADDR0[113]	PP1_A113	FLASH Address[113]
FL_ADDR0[114]	PP1_A114	FLASH Address[114]
FL_ADDR0[115]	PP1_A115	FLASH Address[115]
FL_ADDR0[116]	PP1_A116	FLASH Address[116]
FL_ADDR0[117]	PP1_A117	FLASH Address[117]
FL_ADDR0[118]	PP1_A118	FLASH Address[118]
FL_ADDR0[119]	PP1_A119	FLASH Address[119]
FL_ADDR0[120]	PP1_A120	FLASH Address[120]
FL_ADDR0[121]	PP1_A121	FLASH Address[121]
FL_ADDR0[122]	PP1_A122	FLASH Address[122]
FL_ADDR0[123]	PP1_A123	FLASH Address[123]
FL_ADDR0[124]	PP1_A124	FLASH Address[124]
FL_ADDR0[125]	PP1_A125	FLASH Address[125]
FL_ADDR0[126]	PP1_A126	FLASH Address[126]
FL_ADDR0[127]	PP1_A127	FLASH Address[127]
FL_ADDR0[128]	PP1_A128	FLASH Address[128]
FL_ADDR0[129]	PP1_A129	FLASH Address[129]
FL_ADDR0[130]	PP1_A130	FLASH Address[130]
FL_ADDR0[131]	PP1_A131	FLASH Address[131]
FL_ADDR0[132]	PP1_A132	FLASH Address[132]
FL_ADDR0[133]	PP1_A133	FLASH Address[133]
FL_ADDR0[134]	PP1_A134	FLASH Address[134]
FL_ADDR0[135]	PP1_A135	FLASH Address[135]
FL_ADDR0[136]	PP1_A136	FLASH Address[136]
FL_ADDR0[137]	PP1_A137	FLASH Address[137]
FL_ADDR0[138]	PP1_A138	FLASH Address[138]
FL_ADDR0[139]	PP1_A139	FLASH Address[139]
FL_ADDR0[140]	PP1_A140	FLASH Address[140]
FL_ADDR0[141]	PP1_A141	FLASH Address[141]
FL_ADDR0[142]	PP1_A142	FLASH Address[142]
FL_ADDR0[143]	PP1_A143	FLASH Address[143]
FL_ADDR0[144]	PP1_A144	FLASH Address[144]
FL_ADDR0[145]	PP1_A145	FLASH Address[145]
FL_ADDR0[146]	PP1_A146	FLASH Address[146]
FL_ADDR0[147]	PP1_A147	FLASH Address[147]
FL_ADDR0[148]	PP1_A148	FLASH Address[148]
FL_ADDR0[149]	PP1_A149	FLASH Address[149]
FL_ADDR0[150]	PP1_A150	FLASH Address[150]
FL_ADDR0[151]	PP1_A151	FLASH Address[151]
FL_ADDR0[152]	PP1_A152	FLASH Address[152]
FL_ADDR0[153]	PP1_A153	FLASH Address[153]
FL_ADDR0[154]	PP1_A154	FLASH Address[154]
FL_ADDR0[155]	PP1_A155	FLASH Address[155]
FL_ADDR0[156]	PP1_A156	FLASH Address[156]
FL_ADDR0[157]	PP1_A157	FLASH Address[157]
FL_ADDR0[158]	PP1_A158	FLASH Address[158]
FL_ADDR0[159]	PP1_A159	FLASH Address[159]
FL_ADDR0[160]	PP1_A160	FLASH Address[160]
FL_ADDR0[161]	PP1_A161	FLASH Address[161]
FL_ADDR0[162]	PP1_A162	FLASH Address[162]
FL_ADDR0[163]	PP1_A163	FLASH Address[163]
FL_ADDR0[164]	PP1_A164	FLASH Address[164]
FL_ADDR0[165]	PP1_A165	FLASH Address[165]
FL_ADDR0[166]	PP1_A166	FLASH Address[166]
FL_ADDR0[167]	PP1_A167	FLASH Address[167]
FL_ADDR0[168]	PP1_A168	FLASH Address[168]
FL_ADDR0[169]	PP1_A169	FLASH Address[169]
FL_ADDR0[170]	PP1_A170	FLASH Address[170]
FL_ADDR0[171]	PP1_A171	FLASH Address[171]
FL_ADDR0[172]	PP1_A172	FLASH Address[172]
FL_ADDR0[173]	PP1_A173	FLASH Address[173]
FL_ADDR0[174]	PP1_A174	FLASH Address[174]
FL_ADDR0[175]	PP1_A175	FLASH Address[175]
FL_ADDR0[176]	PP1_A176	FLASH Address[176]
FL_ADDR0[177]	PP1_A177	FLASH Address[177]
FL_ADDR0[178]	PP1_A178	FLASH Address[178]
FL_ADDR0[179]	PP1_A179	FLASH Address[179]
FL_ADDR0[180]	PP1_A180	FLASH Address[180]
FL_ADDR0[181]	PP1_A181	FLASH Address[181]
FL_ADDR0[182]	PP1_A182	FLASH Address[182]
FL_ADDR0[183]	PP1_A183	FLASH Address[183]
FL_ADDR0[184]	PP1_A184	FLASH Address[184]
FL_ADDR0[185]	PP1_A185	FLASH Address[185]
FL_ADDR0[186]	PP1_A186	FLASH Address[186]
FL_ADDR0[187]	PP1_A187	FLASH Address[187]
FL_ADDR0[188]	PP1_A188	FLASH Address[188]
FL_ADDR0[189]	PP1_A189	FLASH Address[189]
FL_ADDR0[190]	PP1_A190	FLASH Address[190]
FL_ADDR0[191]	PP1_A191	FLASH Address[191]
FL_ADDR0[192]	PP1_A192	FLASH Address[192]
FL_ADDR0[193]	PP1_A193	FLASH Address[193]
FL_ADDR0[194]	PP1_A194	FLASH Address[194]
FL_ADDR0[195]	PP1_A195	FLASH Address[195]
FL_ADDR0[196]	PP1_A196	FLASH Address[196]
FL_ADDR0[197]	PP1_A197	FLASH Address[197]
FL_ADDR0[198]	PP1_A198	FLASH Address[198]
FL_ADDR0[199]	PP1_A199	FLASH Address[199]
FL_ADDR0[200]	PP1_A200	FLASH Address[200]
FL_ADDR0[201]	PP1_A201	FLASH Address[201]
FL_ADDR0[202]	PP1_A202	FLASH Address[202]
FL_ADDR0[203]	PP1_A203	FLASH Address[203]
FL_ADDR0[204]	PP1_A204	FLASH Address[204]
FL_ADDR0[205]	PP1_A205	FLASH Address[205]
FL_ADDR0[206]	PP1_A206	FLASH Address[206]
FL_ADDR0[207]	PP1_A207	FLASH Address[207]
FL_ADDR0[208]	PP1_A208	FLASH Address[208]
FL_ADDR0[209]	PP1_A209	FLASH Address[209]
FL_ADDR0[210]	PP1_A210	FLASH Address[210]
FL_ADDR0[211]	PP1_A211	FLASH Address[211]
FL_ADDR0[212]	PP1_A212	FLASH Address[212]
FL_ADDR0[213]	PP1_A213	FLASH Address[213]
FL_ADDR0[214]	PP1_A214	FLASH Address[214]
FL_ADDR0[215]	PP1_A215	FLASH Address[215]
FL_ADDR0[216]	PP1_A216	FLASH Address[216]
FL_ADDR0[217]	PP1_A217	FLASH Address[217]
FL_ADDR0[218]	PP1_A218	FLASH Address[218]
FL_ADDR0[219]	PP1_A219	FLASH Address[219]
FL_ADDR0[220]	PP1_A220	FLASH Address[220]
FL_ADDR0[221]	PP1_A221	FLASH Address[221]
FL_ADDR0[222]	PP1_A222	FLASH Address[222]
FL_ADDR0[223]	PP1_A223	FLASH Address[223]
FL_ADDR0[224]	PP1_A224	FLASH Address[224]
FL_ADDR0[225]	PP1_A225	FLASH Address[225]
FL_ADDR0[226]	PP1_A226	FLASH Address[226]
FL_ADDR0[227]	PP1_A227	FLASH Address[227]
FL_ADDR0[228]	PP1_A228	FLASH Address[228]
FL_ADDR0[229]	PP1_A229	FLASH Address[229]
FL_ADDR0[230]	PP1_A230	FLASH Address[230]
FL_ADDR0[231]	PP1_A231	FLASH Address[231]
FL_ADDR0[232]	PP1_A232	FLASH Address[232]
FL_ADDR0[233]	PP1_A233	FLASH Address[233]
FL_ADDR0[234]	PP1_A234	FLASH Address[234]
FL_ADDR0[235]	PP1_A235	FLASH Address[235]
FL_ADDR0[236]	PP1_A236	FLASH Address[236]
FL_ADDR0[237]	PP1_A237	FLASH Address[237]
FL_ADDR0[238]	PP1_A238	FLASH Address[238]
FL_ADDR0[239]	PP1_A239	FLASH Address[239]
FL_ADDR0[240]	PP1_A240	FLASH Address[240]
FL_ADDR0[241]	PP1_A241	FLASH Address[241]
FL_ADDR0[242]	PP1_A242	FLASH Address[242]
FL_ADDR0[243]	PP1_A243	FLASH Address[243]
FL_ADDR0[244]	PP1_A244	FLASH Address[244]
FL_ADDR0[245]	PP1_A245	FLASH Address[245]
FL_ADDR0[246]	PP1_A246	FLASH Address[246]
FL_ADDR0[247]	PP1_A247	FLASH Address[247]
FL_ADDR0[248]	PP1_A248	FLASH Address[248]
FL_ADDR0[249]	PP1_A249	FLASH Address[249]
FL_ADDR0[250]	PP1_A250	FLASH Address[250]
FL_ADDR0[251]	PP1_A251	FLASH Address[251]
FL_ADDR0[252]	PP1_A252	FLASH Address[252]
FL_ADDR0[253]	PP1_A253	FLASH Address[253]
FL_ADDR0[254]	PP1_A254	FLASH Address[254]
FL_ADDR0[255]	PP1_A255	FLASH Address[255]
FL_ADDR0[256]	PP1_A256	FLASH Address[256]
FL_ADDR0[257]	PP1_A257	FLASH Address[257]
FL_ADDR0[258]	PP1_A258	FLASH Address[258]
FL_ADDR0[259]	PP1_A259	FLASH Address[259]
FL_ADDR0[260]	PP1_A260	FLASH Address[260]
FL_ADDR0[261]	PP1_A261	FLASH Address[261]
FL_ADDR0[262]	PP1_A262	FLASH Address[262]
FL_ADDR0[263]	PP1_A263	FLASH Address[263]
FL_ADDR0[264]	PP1_A264	FLASH Address[264]
FL_ADDR0[265]	PP1_A265	FLASH Address[265]
FL_ADDR0[266]	PP1_A266	FLASH Address[266]
FL_ADDR0[267]	PP1_A267	FLASH Address[267]
FL_ADDR0[268]	PP1_A268	FLASH Address[268]
FL_ADDR0[269]	PP1_A269	FLASH Address[269]
FL_ADDR0[270]	PP1_A270	FLASH Address[270]
FL_ADDR0[271]	PP1_A271	FLASH Address[271]
FL_ADDR0[272]	PP1_A272	FLASH Address[272]
FL_ADDR0[273]	PP1_A273	FLASH Address[273]
FL_ADDR0[274]	PP1_A274	FLASH Address[274]
FL_ADDR0[275]	PP1_A275	FLASH Address[275]
FL_ADDR0[276]	PP1_A276	FLASH Address[276]
FL_ADDR0[277]	PP1_A277	FLASH Address[277]
FL_ADDR0[278]	PP1_A278	FLASH Address[278]
FL_ADDR0[279]	PP1_A279	FLASH Address[279]
FL_ADDR0[280]	PP1_A280	FLASH Address[280]
FL_ADDR0[281]	PP1_A281	FLASH Address[281]
FL_ADDR0[282]	PP1_A282	FLASH Address[282]
FL_ADDR0[283]	PP1_A283	FLASH Address[283]
FL_ADDR0[284]	PP1_A284	FLASH Address[284]
FL_ADDR0[285]	PP1_A285	FLASH Address[285]
FL_ADDR0[286]	PP1_A286	FLASH Address[286]
FL_ADDR0[287]	PP1_A287	FLASH Address[287]
FL_ADDR0[288]	PP1_A288	FLASH Address[288]
FL_ADDR0[289]	PP1_A289	FLASH Address[289]
FL_ADDR0[290]	PP1_A290	FLASH Address[290]
FL_ADDR0[291]	PP1_A291	FLASH Address[291]
FL_ADDR0[292]	PP1_A292	FLASH Address[292]
FL_ADDR0[293]	PP1_A293	FLASH Address[293]
FL_ADDR0[294]	PP1_A294	FLASH Address[294]
FL_ADDR0[295]	PP1_A295	FLASH Address[295]
FL_ADDR0[296]	PP1_A296	FLASH Address[296]
FL_ADDR0[297]	PP1_A297	FLASH Address[297]
FL_ADDR0[298]	PP1_A298	FLASH Address[298]
FL_ADDR0[299]	PP1_A299	FLASH Address[299]
FL_ADDR0[300]	PP1_A300	FLASH Address[300]
FL_ADDR0[301]	PP1_A301	FLASH Address[301]
FL_ADDR0[302]	PP1_A302	FLASH Address[302]
FL_ADDR0[303]	PP1_A303	FLASH Address[303]
FL_ADDR0[304]	PP1_A304	FLASH Address[304]
FL_ADDR0[305]	PP1_A305	FLASH Address[305]
FL_ADDR0[306]	PP1_A306	FLASH Address[306]
FL_ADDR0[307]	PP1_A307	FLASH Address[307]
FL_ADDR0[308]	PP1_A308	FLASH Address[308]
FL_ADDR0[309]	PP1_A309	FLASH Address[309]
FL_ADDR0[310]	PP1_A310	FLASH Address[310]
FL_ADDR0[311]	PP1_A311	FLASH Address[311]
FL_ADDR0[312]	PP1_A312	FLASH Address[312]
FL_ADDR0[313]	PP1_A313	FLASH Address[313]
FL_ADDR0[314]	PP1_A314	FLASH Address[314]
FL_ADDR0[315]	PP1_A315	FLASH Address[315]
FL_ADDR0[316]	PP1_A316	FLASH Address[316]
FL_ADDR0[317]	PP1_A317	FLASH Address[317]
FL_ADDR0[318]	PP1_A318	FLASH Address[318]
FL_ADDR0[319]	PP1_A319	FLASH Address[319]
FL_ADDR0[320]	PP1_A320	FLASH Address[320]
FL_ADDR0[321]	PP1_A321	FLASH Address[321]
FL_ADDR0[322]	PP1_A322	FLASH Address[322]
FL_ADDR0[323]	PP1_A323	FLASH Address[323]
FL_ADDR0[324]	PP1_A324	FLASH Address[324]
FL_ADDR0[325]	PP1_A325	FLASH Address[325]
FL_ADDR0[326]	PP1_A326	FLASH Address[326]
FL_ADDR0[327]	PP1_A327	FLASH Address[327]
FL_ADDR0[328]	PP1_A328	FLASH Address[328]
FL_ADDR0[329]	PP1_A329	FLASH Address[329]
FL_ADDR0[330]	PP1_A330	FLASH Address[330]
FL_ADDR0[331]	PP1_A331	FLASH Address[331]
FL_ADDR0[332]	PP1_A332	FLASH Address[332]
FL_ADDR0[333]	PP1_A333	FLASH Address[333]

HEX3[5]	PIN_U22	Seven Segment Digit 3[5]
HEX3[6]	PIN_W24	Seven Segment Digit 3[6]
HEX4[0]	PIN_U9	Seven Segment Digit 4[0]
HEX4[1]	PIN_U1	Seven Segment Digit 4[1]
HEX4[2]	PIN_U2	Seven Segment Digit 4[2]
HEX4[3]	PIN_T4	Seven Segment Digit 4[3]
HEX4[4]	PIN_R7	Seven Segment Digit 4[4]
HEX4[5]	PIN_R6	Seven Segment Digit 4[5]
HEX4[6]	PIN_T3	Seven Segment Digit 4[6]
HEX5[0]	PIN_T2	Seven Segment Digit 5[0]
HEX5[1]	PIN_P6	Seven Segment Digit 5[1]
HEX5[2]	PIN_P7	Seven Segment Digit 5[2]
HEX5[3]	PIN_T9	Seven Segment Digit 5[3]
HEX5[4]	PIN_R5	Seven Segment Digit 5[4]
HEX5[5]	PIN_R4	Seven Segment Digit 5[5]
HEX5[6]	PIN_R3	Seven Segment Digit 5[6]
HEX6[0]	PIN_R2	Seven Segment Digit 6[0]
HEX6[1]	PIN_P4	Seven Segment Digit 6[1]
HEX6[2]	PIN_P3	Seven Segment Digit 6[2]
HEX6[3]	PIN_M2	Seven Segment Digit 6[3]
HEX6[4]	PIN_M3	Seven Segment Digit 6[4]
HEX6[5]	PIN_M5	Seven Segment Digit 6[5]
HEX6[6]	PIN_M4	Seven Segment Digit 6[6]
HEX7[0]	PIN_L3	Seven Segment Digit 7[0]
HEX7[1]	PIN_L2	Seven Segment Digit 7[1]
HEX7[2]	PIN_L9	Seven Segment Digit 7[2]
HEX7[3]	PIN_L6	Seven Segment Digit 7[3]
HEX7[4]	PIN_L7	Seven Segment Digit 7[4]
HEX7[5]	PIN_P9	Seven Segment Digit 7[5]
HEX7[6]	PIN_N9	Seven Segment Digit 7[6]
Signal Name	FPGA Pin No.	Description

Physical Pins of FPGA

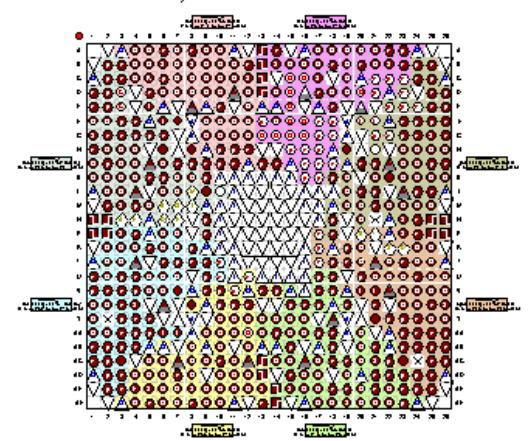


On the “compiler” / “programmer”

Quartus II - C:/Documents and Settings/LIP/Desktop/DE2_Sound/DE2_Sound/DE2_Default - DE2_Default - [Pin Planner]

File Edit View Processing Tools Window

Top View - Wire Bond
Cyclone II - EP2C35F672C6



Named:	Node Name	Direction	Location	I/O Bank	VREF Group	I/O Standard	Reserved
1	AUD_ADCDAT	Input	PIN_B5	3	B3_N1	3.3-V LVTTTL	
2	AUD_ADCLCK	Output	PIN_C5	3	B3_N1	3.3-V LVTTTL	
3	AUD_BCLK	Output	PIN_B4	3	B3_N1	3.3-V LVTTTL	
4	AUD_DACDAT	Output	PIN_A4	3	B3_N1	3.3-V LVTTTL	
5	AUD_DACLCK	Output	PIN_C6	3	B3_N1	3.3-V LVTTTL	
6	AUD_XCK	Output	PIN_A5	3	B3_N1	3.3-V LVTTTL	
7	CLOCK_27	Input	PIN_D13	3	B3_N0	3.3-V LVTTTL (default)	
8	CLOCK_50	Input	PIN_N2	2	B2_N1	3.3-V LVTTTL (default)	
9	DRAM_ADDR[11]	Output	PIN_V5	1	B1_N1	3.3-V LVTTTL (default)	
10	DRAM_ADDR[10]	Output	PIN_Y1	1	B1_N1	3.3-V LVTTTL (default)	
11	DRAM_ADDR[9]	Output	PIN_W3	1	B1_N1	3.3-V LVTTTL (default)	
12	DRAM_ADDR[8]	Output	PIN_W4	1	B1_N1	3.3-V LVTTTL (default)	
13	DRAM_ADDR[7]	Output	PIN_U5	1	B1_N1	3.3-V LVTTTL (default)	
14	DRAM_ADDR[6]	Output	PIN_U7	1	B1_N1	3.3-V LVTTTL (default)	
15	DRAM_ADDR[5]	Output	PIN_U6	1	B1_N1	3.3-V LVTTTL (default)	
16	DRAM_ADDR[4]	Output	PIN_W1	1	B1_N0	3.3-V LVTTTL (default)	

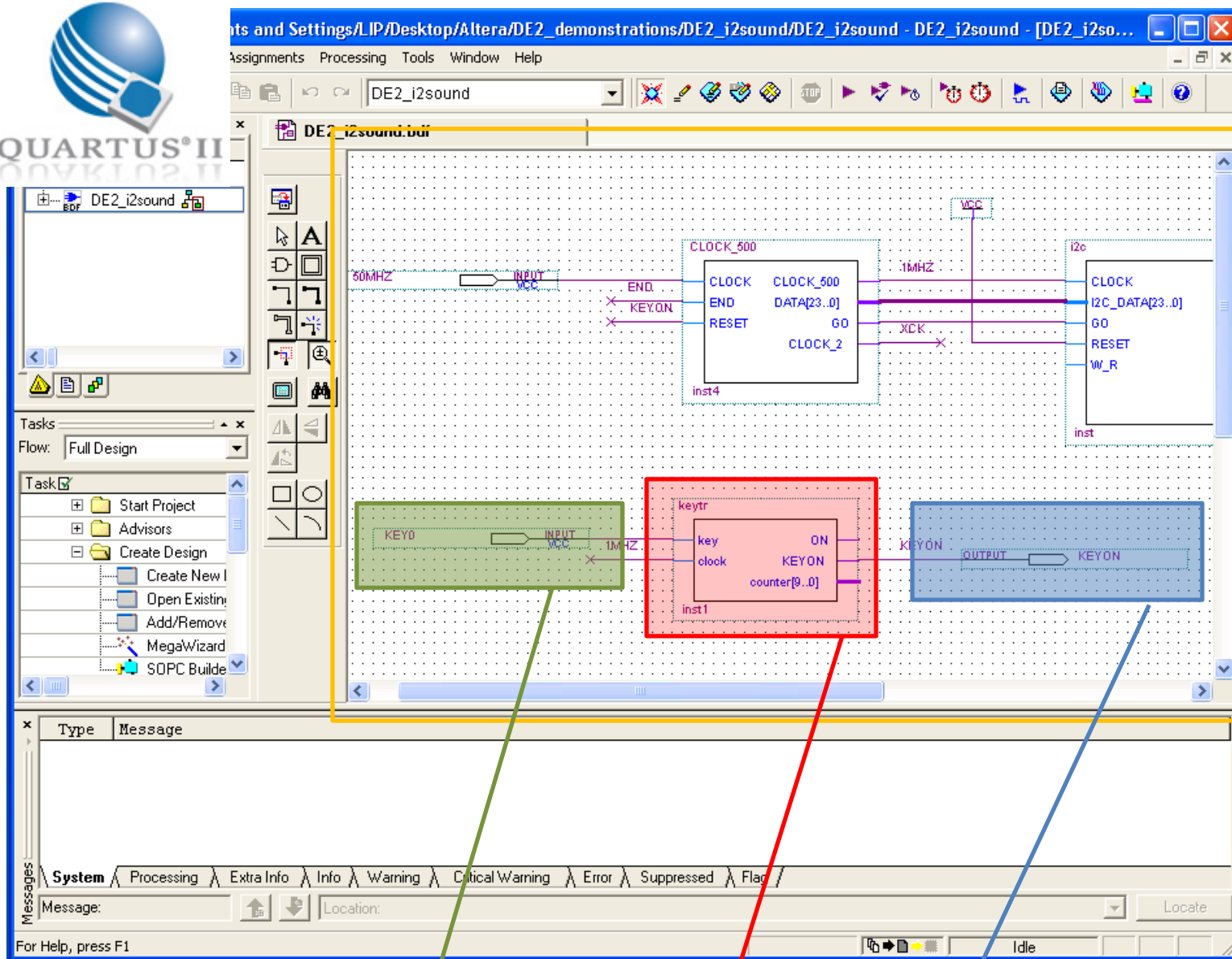
For Help, press F1

Friendly Name

Physical Names



QUARTUS® II



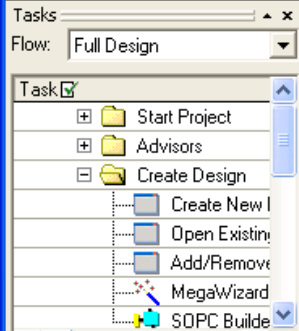
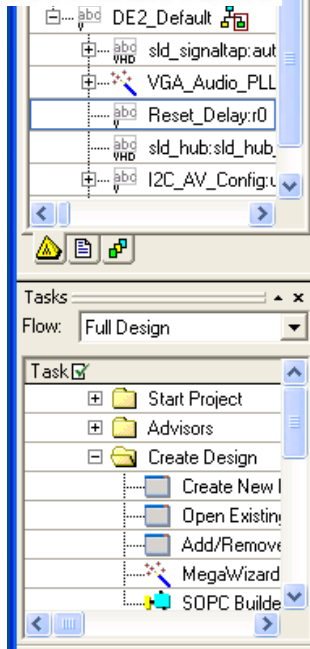
Input

Lógica

Output



QUARTUS II



```

1 module Reset_Delay(iCLK,oRESET);
2   input iCLK;
3   output reg oRESET;
4   reg [19:0] Cont;
5
6   always@(posedge iCLK)
7   begin
8     if(Cont!=20'hFFFFFF)
9     begin
10      Cont    <= Cont+1;
11      oRESET  <= 1'b0;
12    end
13    else
14      oRESET  <= 1'b1;
15  end
16
17 endmodule
    
```

Programação
esquemático

Input

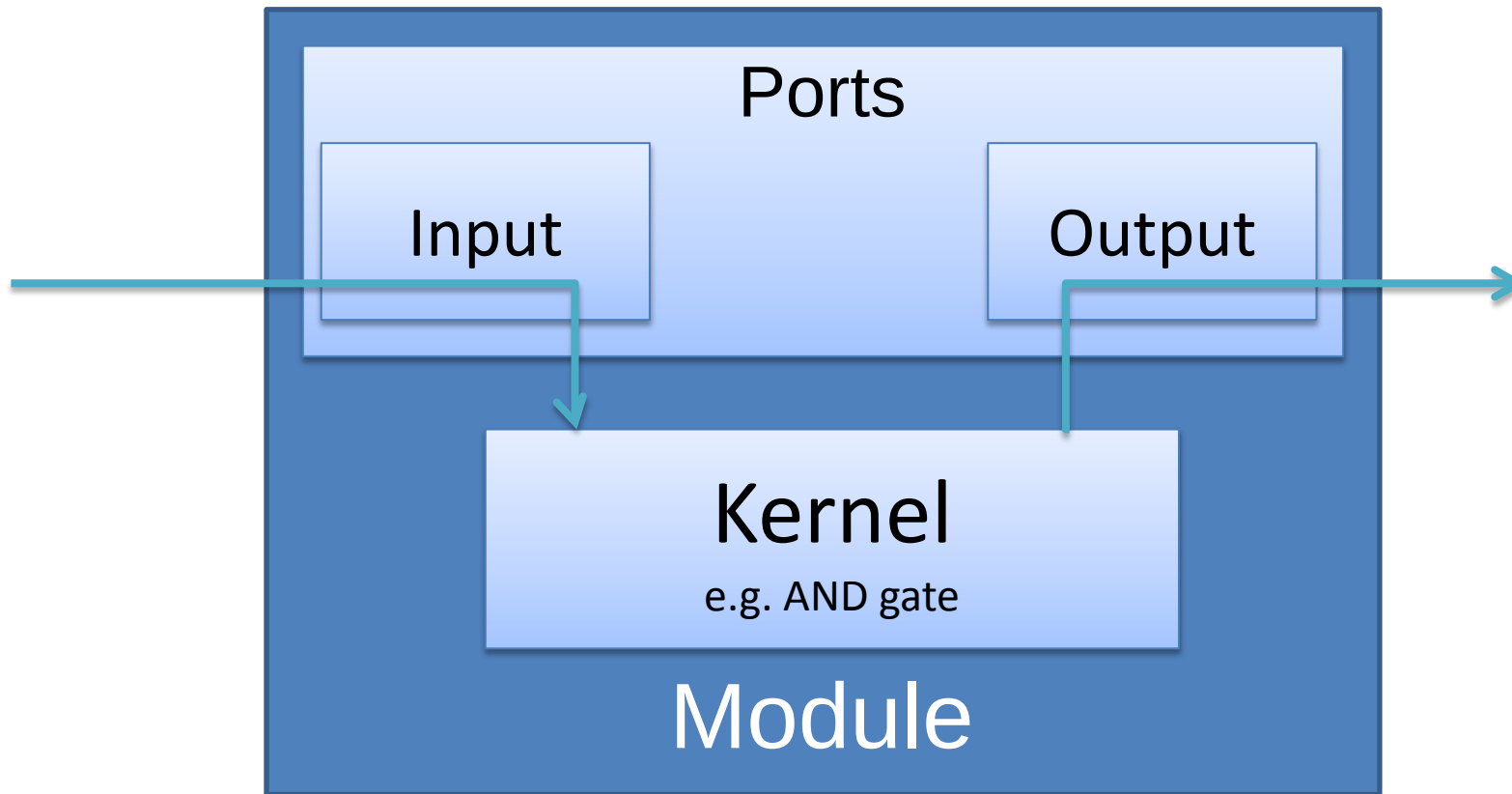
Output

Lógica

Structuring... Modules

Modules are the building blocks in Verilog!

There is at least one module: The top one that has the name of the project!



Ports in the top level module link directly to the pins

Now, the text you need to write that the compiler will interpret with the configuration for the FPGA to do what you want.
a.k.a. code

```
module mux(input a,b,sel, output q, qbar);  
  wire selbar, q1, q2;  
  not n1(selbar, sel);  
  and a1(q1, a, selbar);  
  and a2(q2, b, sel);  
  or o1(q, q1, q2);  
  not n2(qbar, q)  
endmodule
```

Selbar, q1, q2 are names
given to wires

not, and, or are modules!
n1, a1, a2, o1, n2 are
names of instances

Another way...

```
module mux(input a,b,sel, output q, qbar);
```

```
    assign q = sel? a : b;  
    assign qbar = ~ q;
```

```
endmodule
```

Same as
If (sel) then a else b

Assign means that
Left Hand Side (LHS)
of '=' takes 'immediately' the value that results from
Right Hand Side (RHS)

Yet another way...

Notice the **reg** keyword...

```
module mux(input a,b,sel, output reg q, qbar);
```

```
    always @ (a,b,sel) begin
```

```
        if (sel) q=a;
```

```
        else q=b;
```

```
    end
```

```
    assign qbar = ~ q;
```

```
endmodule
```

"Whenever a,b or sel changes"

Can be replaced by
always @ (*)

"Whenever anything changes"

If and cases can be used

Verilog data values

Value	Meaning
0	Logic zero, “Low”
1	Logic one, “High”
Z or ?	High Impedance (tri-state)
X	Unknow (simulation)

Numeric constants

Full format: <Width>'<Radix>value

Width: number

Radix: d=decimal, h=hex, o=ocatl, b=binary

Value	Meaning
123	Default: decimal radix
'd123	'd=decimal radix
'h7B	'h=hexadecimal radix
'o173	'o=ocatl radix
'b111_101	'b=binary radix
16'b11111	A binary with 16 bits
16'd5	A 16 bit decimal = 'b0000_0000_0000_0101

How many bits?

Wire ab;	A 1 bit wire called <u>ab</u>
Wire ab,cd;	Two 1 bit wires called <u>ab</u> and <u>cd</u>
wire [31:0] ef;	A 32 bits wire bus called <u>ef</u> ;
{ab,cd}	Concatenation of <u>ab</u> and <u>cd</u> ;
ef[15]	Bit #15 (the sixteenth) of <u>ef</u>
ef[7:0]	First 8 bits of <u>ef</u> (the ones to the right)

What does this means?

```
wire [31:0] kk;  
Wire [7:0] a,b,c,d;  
Assign kk={d,c,b,a}
```

Boolean operators

- **Bitwise operators** perform bit-oriented operations on vectors
 - $\sim(4'b0101) = \{\sim 0, \sim 1, \sim 0, \sim 1\} = 4'b1010$
 - $4'b0101 \& 4'b0011 = \{0\&0, 1\&0, 0\&1, 1\&1\} = 4'b0001$
- **Reduction operators** act on each bit of a single input vector
 - $\&(4'b0101) = 0 \& 1 \& 0 \& 1 = 1'b0$
- **Logical operators** return one-bit (true/false) results
 - $!(4'b0101) = 1'b0$

Bitwise

$\sim a$	NOT
$a \& b$	AND
$a b$	OR
$a \wedge b$	XOR
$a \sim\wedge b$ $a \wedge\sim b$	XNOR

Reduction

$\&a$	AND
$\sim\&a$	NAND
$ a$	OR
$\sim a$	NOR
$\wedge a$	XOR
$\sim\wedge a$ $\wedge\sim a$	XNOR

Logical

$!a$	NOT
$a \&\& b$	AND
$a b$	OR
$a == b$ $a != b$	[in]equality returns x when x or z in bits. Else returns 0 or 1
$a === b$ $a !== b$	case [in]equality returns 0 or 1 based on bit by bit comparison

*Note distinction between $\sim a$ and $!a$
when operating on multi-bit values*

Other operators

Conditional

$a ? b : c$	If a then b else c
-------------	--------------------

Relational

$a > b$	greater than
$a \geq b$	greater than or equal
$a < b$	Less than
$a \leq b$	Less than or equal

Arithmetic

$-a$	negate
$a + b$	add
$a - b$	subtract
$a * b$	multiply
a / b	divide
$a \% b$	modulus
$a ** b$	exponentiate
$a \ll b$	logical left shift
$a \gg b$	logical right shift
$a \lll b$	arithmetic left shift
$a \ggg b$	arithmetic right shift

And now our lab session...

Two simple exercises:

- 1) “OLA MUNDO” just play directly with bits
- 2) Make a module that has:
 - Inputs: 4 bits codificam numero binario
 - Ouputs: as 7 linhas de 1 display de 7 segmentos
 - kernel: activar segmentos do display para mostrar número

Helps...

Usign DE2 you get all hardware issues “solved”
DE2_TOP project is a bare project: use it
DE2_TOP already has “friendly names”
DE2_TOP has some assigns... Play with them

File→Open Project→DE2_top

Quartus II - C:/Documents and Settings/LIP/Desktop/Altera/DE2_demonstrations/DE2_Top/DE2_TOP - DE2_TOP - [DE2_TOP.v]

File Edit View Project Assignments Processing Tools Window Help

DE2_TOP

Project Navigator

Entity

Cyclone II: EP2C35F672C6

DE2_TOP

Tasks

Flow: Full Design

Task

- Start Project
- Advisors
- Create Design
- Create New I
- Open Existing
- Add/Remove
- MegaWizard
- SOPC Builder
- Assign Constraint

```
42 // V1.2 :| Johnny Chen :| 05/11/16 :| Fixed ISP1362 INT/
43 // -----
44
45 module DE2_TOP
46
47 // Clock Input
48 CLOCK_27, // 27 MHz
49 CLOCK_50, // 50 MHz
50 EXT_CLOCK, // External Clock
51 // Push Button
52 KEY, // Pushbutton[3:0]
53 // DPDT Switch
54 SW, // Toggle Switch[17:0]
55 // 7-SEG Display
56 HEX0, // Seven Segment Digit 0
57 HEX1, // Seven Segment Digit 1
58 HEX2, // Seven Segment Digit 2
59 HEX3, // Seven Segment Digit 3
60 HEX4, // Seven Segment Digit 4
61 HEX5, // Seven Segment Digit 5
62 HEX6, // Seven Segment Digit 6
63 HEX7, // Seven Segment Digit 7
64 // LED
65 LEDG, // LED Green[8:0]
66 LEDR, // LED Red[17:0]
67 // UART
68 UART_TXD, // UART Transmitter
69 UART_RXD, // UART Receiver
```

Messages

System Processing Extra Info Info Warning Critical Warning Error Suppressed Flag

Message:

Location:

For Help, press F1

start

```
174 // Clock Input
175 input CLOCK_27; // 27 MHz
176 input CLOCK_50; // 50 MHz
177 input EXT_CLOCK; // External Clock
178 // Push Button
179 input [3:0] KEY; // Pushbutton[3:0]
180 // DPDT Switch
181 input [17:0] SW; // Toggle Switch[17:0]
182 // 7-SEG Display
183 output [6:0] HEX0; // Seven Segment Digit 0
184 output [6:0] HEX1; // Seven Segment Digit 1
185 output [6:0] HEX2; // Seven Segment Digit 2
186 output [6:0] HEX3; // Seven Segment Digit 3
187 output [6:0] HEX4; // Seven Segment Digit 4
188 output [6:0] HEX5; // Seven Segment Digit 5
189 output [6:0] HEX6; // Seven Segment Digit 6
190 output [6:0] HEX7; // Seven Segment Digit 7
191 // LED
192 output [8:0] LEDG; // LED Green[8:0]
193 output [17:0] LEDR; // LED Red[17:0]
194 // UART
195 output UART_TXD; // UART Transmitter
196 input UART_RXD; // UART Receiver
197 // IRDA
198 output IRDA_TXD; // IRDA Transmitter
199 input IRDA_RXD; // IRDA Receiver
200 // SDRAM Interface
201 inout [15:0] DRAM_DQ; // SDRAM Data bus 16 Bits
202 output [11:0] DRAM_ADDR; // SDRAM Address bus 12 Bits
```

```
300 // Turn on all display
301 assign HEX0 = 7'h00;
302 assign HEX1 = 7'h00;
303 assign HEX2 = 7'h00;
304 assign HEX3 = 7'h00;
305 assign HEX4 = 7'h00;
306 assign HEX5 = 7'h00;
307 assign HEX6 = 7'h00;
308 assign HEX7 = 7'h00;
309 assign LEDG = 9'h1FF;
310 assign LEDR = 18'h3FFFF;
311 assign LCD_ON = 1'b1;
312 assign LCD_BLON = 1'b1;
313
314 // All inout port turn to tri-state
315 assign DRAM_DQ = 16'hzzzz;
316 assign FL_DQ = 8'hzz;
317 assign SRAM_DQ = 16'hzzzz;
318 assign OTG_DATA = 16'hzzzz;
319 assign LCD_DATA = 8'hzz;
320 assign SD_DAT = 1'bz;
321 assign I2C_SDAT = 1'bz;
322 assign ENET_DATA = 16'hzzzz;
323 assign AUD_ADCLRCK = 1'bz;
324 assign AUD_DACLK = 1'bz;
325 assign AUD_BCLK = 1'bz;
326 assign GPIO_0 = 36'hzzzzzzzz;
327 assign GPIO_1 = 36'hzzzzzzzz;
328
```

